5.8- 8.5GHz Power Amplifier

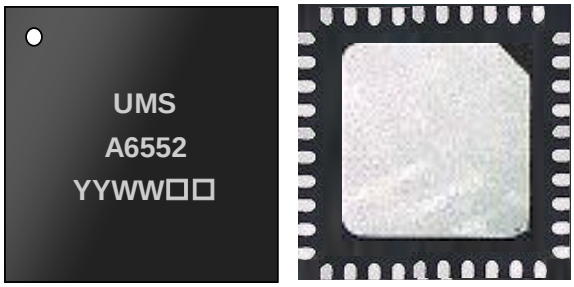
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA6552-QJG is a three stage monolithic GaAs high power circuit producing 4 Watt output power.

It is designed for Point to Point radio and commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.5µm gate length.

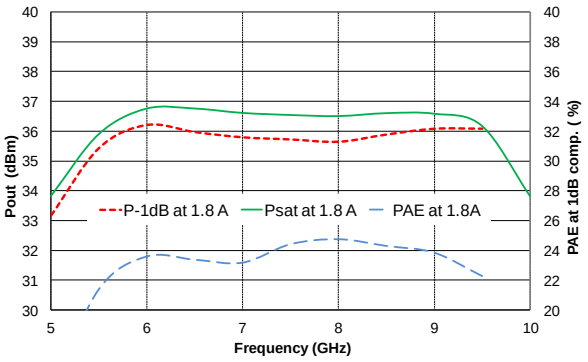
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 5.8- 8.5GHz
- 36dBm saturated power
- 35dBm at 1dB compression
- 22dB gain
- DC bias: Vd = 7.0Volt @ Id = 1.8A
- QFN6x6
- MSL3

Pout & PAE versus frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.8		8.5	GHz
Gain	Linear Gain		22		dB
Psat	Saturated output power		36		dBm
OIP3	Output IP3		45		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +7.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	5.8		8.5	GHz
G	Small Signal Gain		22		dB
ΔG	Gain variation in temperature		+/-0.035		dB/°C
P1dB	Output power @1dB compression		35		dBm
Psat	Saturated output power		36		dBm
OIP3	Output IP3		45		dBm
PAE	PAE at 1dB compression		22		%
Rlin	Input Return Loss		12		dB
Rlout	Output Return Loss		15		dB
Dr (1)	Detection dynamic range		30		dB
Vdetect1	Voltage detection Vref1-Vdet1 up to Psat		5 to 1200		mV
Vdetect2	Voltage detection Vref2-Vdet2 up to Psat		5 to 1200		mV
Vg	DC Gate voltage		-0.4		V
Idet	Detector current		3		mA
Idq	Total quiescent drain current		1800		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

(1) Dr: Output power detection up to Psat.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	7.5	V
Idq	Quiescent drain bias current	2.5	A
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power overdrive (2)	20	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1	13, 38	DC Drain voltage 1st stage	7	V
VD2	16, 35	DC Drain voltage 2nd stage	7	V
VD3	19, 32	DC Drain voltage 3rd stage	7	V
VG1	14, 37	DC Gate voltage 1st & 2nd stage	-0.4	V
VG2	17, 34	DC Gate voltage 3rd stage	-0.4	V
VDC1,2	23, 29	DC Detector biasing voltage	7	V

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.

The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

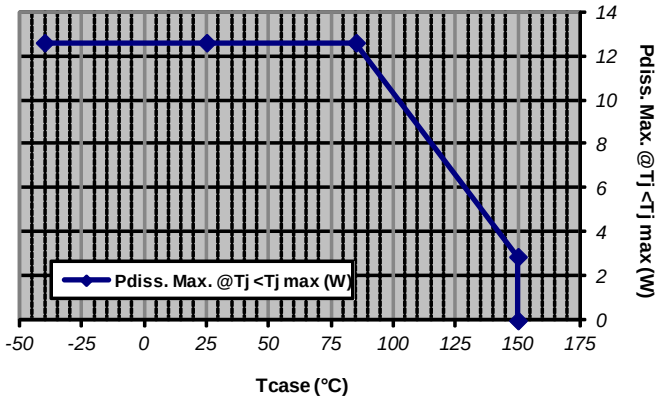
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

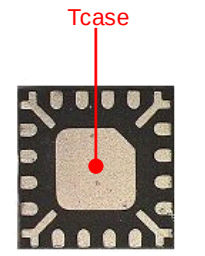
DEVICE THERMAL SPECIFICATION : CHA6552-QJG			
Recommended max. junction temperature (Tj max)	:	169	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	12.6	W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	149	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<6	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	85	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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Typical Package Sij parameters

Tamb.= +25°C, Vd = 7.0V, Id = 1.8A

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-1.041	84.3	-73.211	92.9	-83.863	-99.5	-0.213	-78.1
3.0	-3.099	27.0	-79.988	27.0	-38.552	-141.8	-0.529	-124.7
4.0	-8.054	-28.2	-78.404	53.8	8.536	2.3	-2.347	173.7
5.0	-10.994	-86.6	-69.536	72.4	22.224	87.1	-9.511	114.4
6.0	-14.070	-172.0	-64.590	34.8	23.692	-114.2	-16.277	110.8
7.0	-16.029	122.1	-65.219	2.5	23.443	79.7	-15.341	75.4
8.0	-17.658	84.4	-69.670	16.9	23.387	-74.4	-24.341	-30.5
9.0	-30.015	114.7	-75.711	119.7	23.174	117.7	-12.388	148.4
10.0	-8.525	111.4	-63.313	70.8	17.932	-70.0	-7.272	90.0
11.0	-5.984	49.3	-63.445	-0.8	5.990	124.8	-4.047	46.0
12.0	-5.661	10.0	-68.226	-146.6	-7.531	-14.4	-1.990	2.1
13.0	-5.516	-22.4	-74.097	-143.6	-21.911	-135.2	-1.311	-37.8
14.0	-5.475	-52.5	-53.703	136.3	-35.575	118.5	-1.095	-72.4
15.0	-5.537	-81.2	-48.721	78.7	-45.391	53.2	-1.118	-105.6
16.0	-5.739	-109.6	-44.152	36.3	-44.997	30.4	-1.238	-137.8
17.0	-6.197	-139.6	-40.969	1.2	-40.798	1.3	-1.382	-170.3
18.0	-7.004	-171.5	-41.763	-40.6	-41.908	-40.3	-1.563	154.1
19.0	-8.237	148.2	-45.063	-62.1	-44.861	-61.7	-1.791	117.2
20.0	-9.780	94.5	-44.475	-70.1	-43.960	-70.1	-1.999	78.0
21.0	-9.384	23.6	-42.375	-96.8	-41.484	-100.3	-2.147	38.5
22.0	-6.348	-39.4	-40.298	-104.6	-39.432	-106.6	-2.347	-0.5
23.0	-3.693	-87.0	-38.076	-119.5	-38.272	-120.6	-2.815	-40.5
24.0	-2.177	-125.1	-36.219	-164.4	-36.886	-158.7	-4.565	-81.6
25.0	-1.468	-157.3	-33.529	157.9	-33.718	157.1	-11.243	-105.5
26.0	-1.118	177.2	-31.545	101.8	-31.550	100.4	-11.609	-83.8
27.0	-0.966	154.3	-30.768	45.4	-30.970	47.2	-9.455	-85.6
28.0	-0.776	132.5	-31.409	-39.8	-31.359	-39.6	-5.043	-102.7
29.0	-0.739	112.0	-32.672	-120.4	-32.606	-119.4	-3.694	-140.4
30.0	-0.732	91.6	-34.645	174.8	-34.587	175.0	-4.390	-178.8
31.0	-0.705	72.7	-40.059	98.4	-40.531	98.3	-9.640	130.9
32.0	-0.642	52.1	-45.666	29.0	-46.044	27.5	-18.978	-100.2
33.0	-0.647	30.0	-50.268	-96.0	-53.982	-100.8	-8.681	-139.0
34.0	-0.965	5.5	-42.309	-123.6	-42.891	-127.4	-5.483	-158.1
35.0	-1.638	-24.5	-37.294	161.1	-37.655	159.9	-2.266	176.9
36.0	-2.832	-62.7	-39.019	109.4	-38.476	107.1	-1.273	148.9
37.0	-4.695	-118.1	-43.328	97.5	-42.419	98.7	-0.872	126.2
38.0	-4.952	161.7	-41.831	103.7	-41.328	102.6	-0.678	106.9
39.0	-2.970	95.5	-41.115	75.0	-41.029	71.5	-0.405	89.2
40.0	-1.664	52.2	-40.701	76.5	-40.312	76.1	-0.383	71.2

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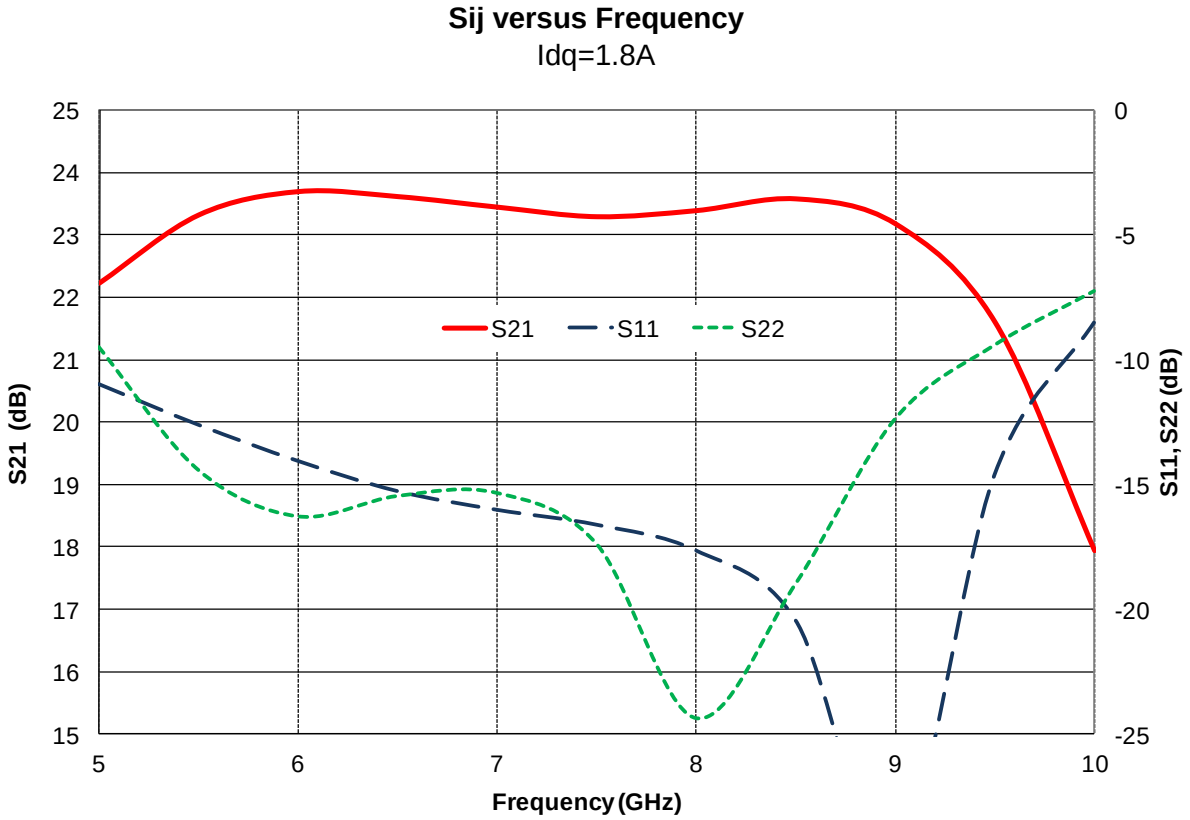
Typical Sij Measurements

Tamb.= +25°C, Vd = +7.0V, Id = 1.8A
Measurement in the plan of the QFN, using a board compatible with RF probes



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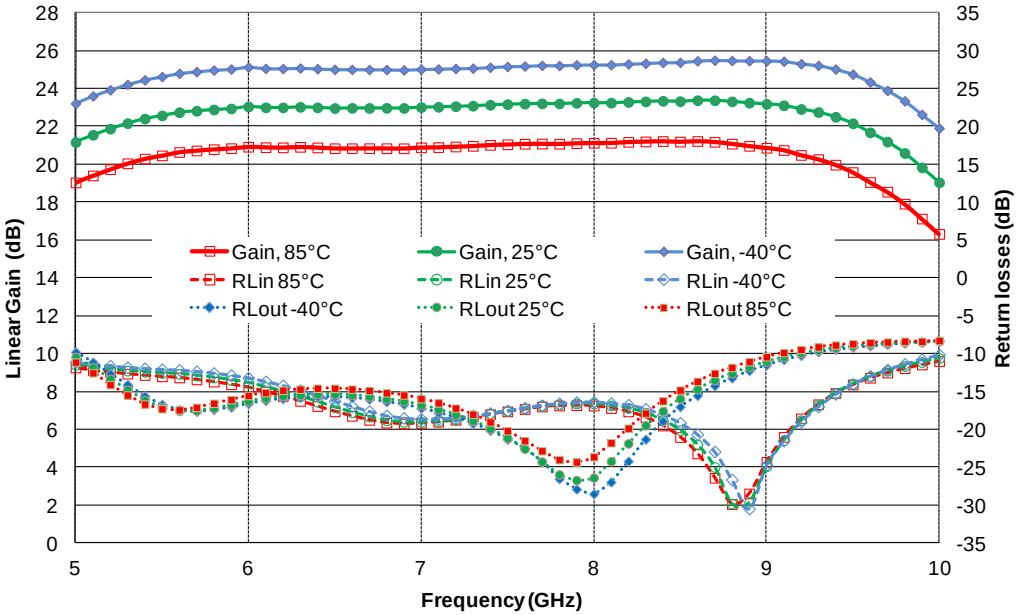
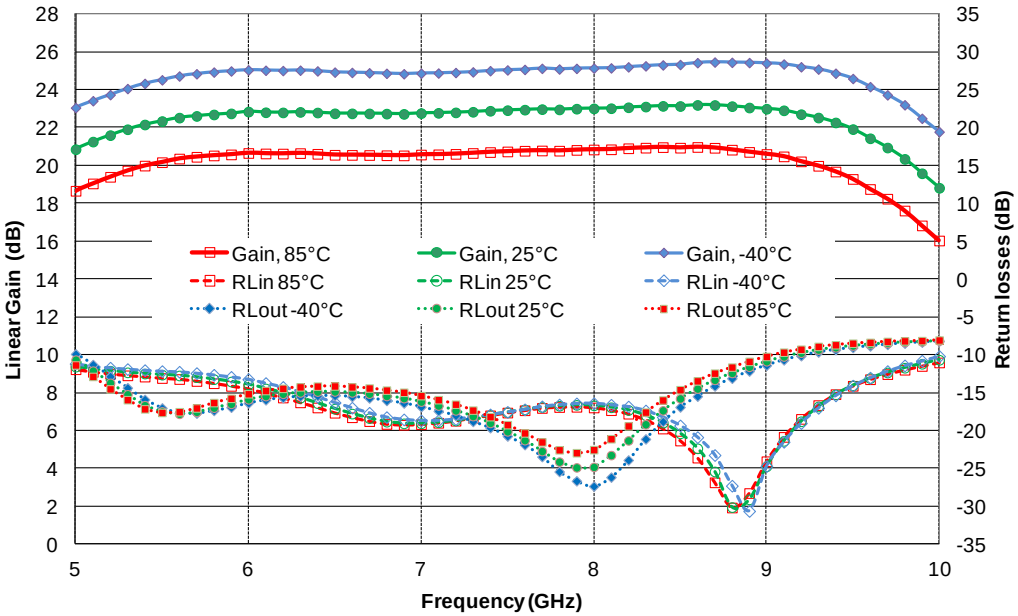
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Id = 1.8A
Measurement in the plan of the QFN, using the proposed land pattern & board, as defined in paragraph “Evaluation mother board”

Linear Gain & Return Losses versus Frequency & Temperature
Idq =1.8A



Linear Gain & Return Losses versus Frequency & Temperature
Idq = 2.0A



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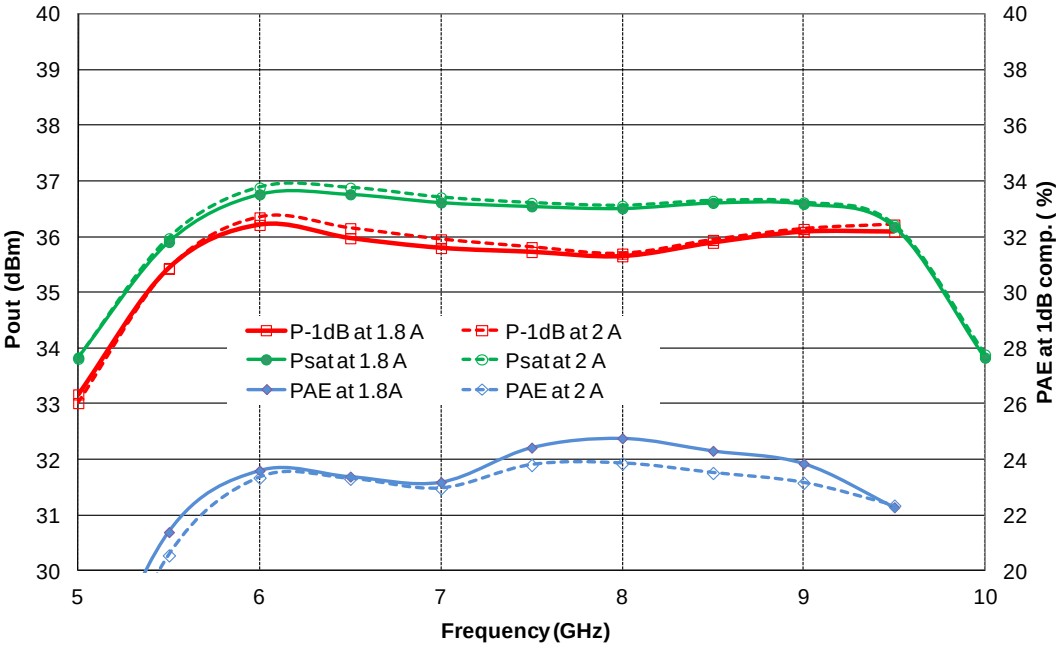
Typical Board Measurements

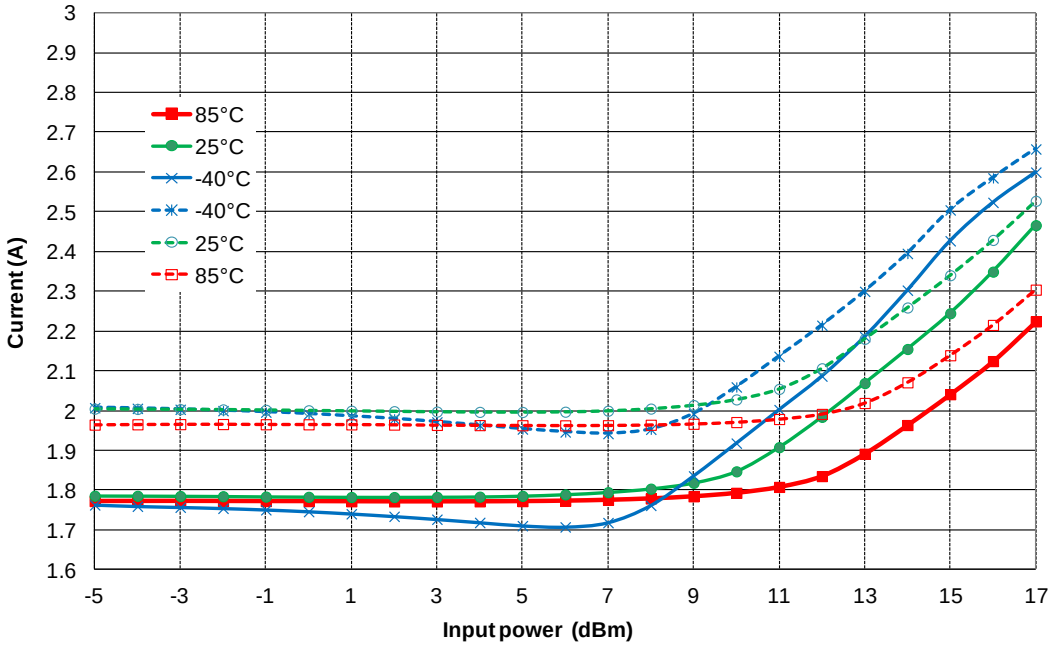
Tamb.= +25°C, Vd = +7.0V, Id = 1.8A

Output Power & PAE versus Frequency & Idq



Current versus Input Power & Temperature

Idq = 1.8A & 2.0A



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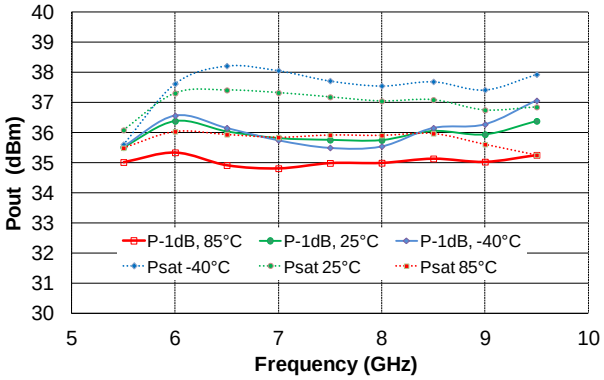
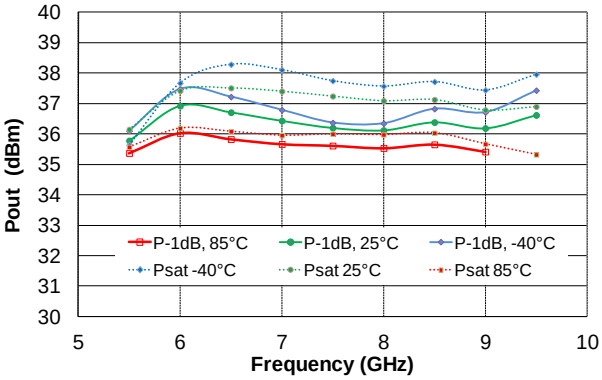
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Id = 1.8A

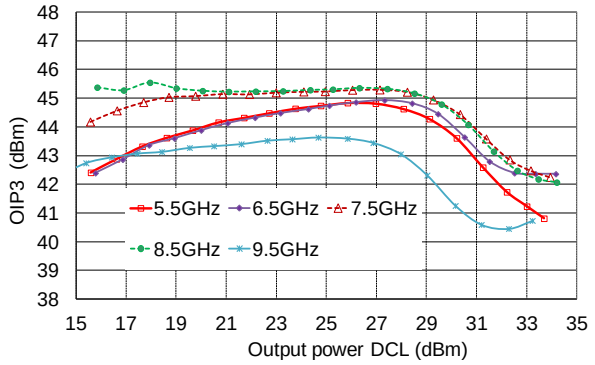
Power versus Frequency & Temperature
Idq = 1.8A



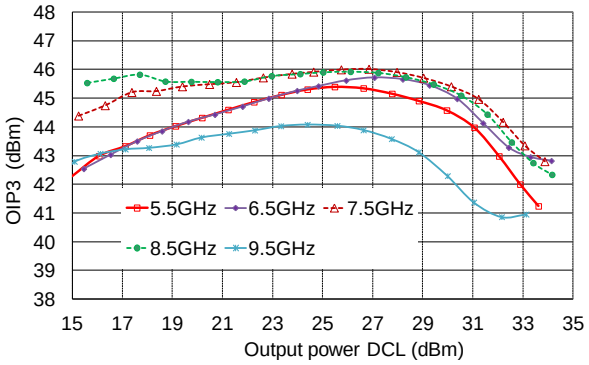
Power versus Frequency & Temperature
Idq = 2.0A



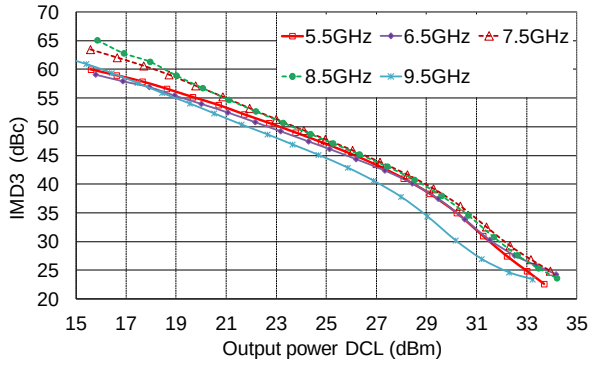
Output IP3 versus Pout & Frequency
Idq = 1.8A



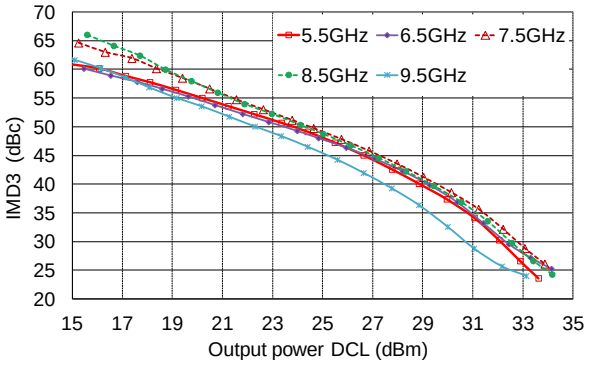
Output IP3 versus Pout & Frequency
Idq = 2.0A



IMD3 versus Pout & Frequency
Idq = 1.8A



IMD3 versus Pout & Frequency
Idq = 2.0A



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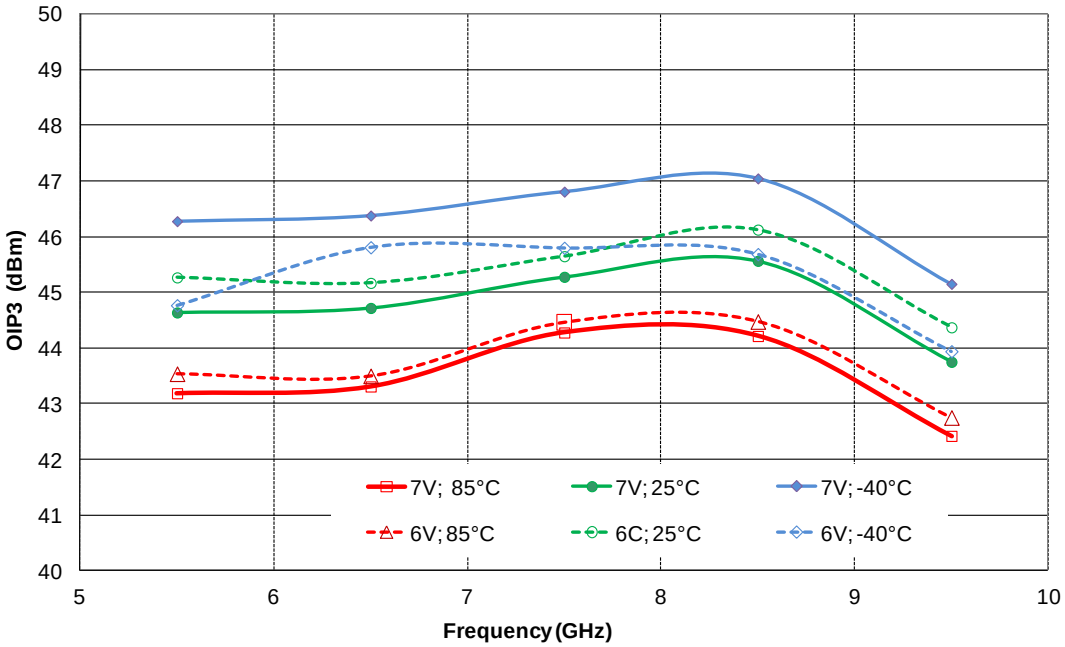
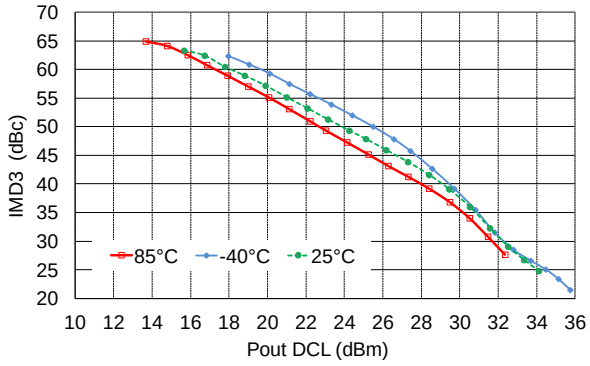
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Id = 1.8A

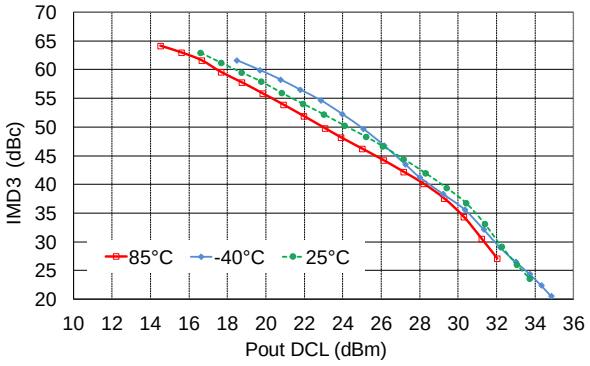
Output IP3 versus Frequency, Temperature & Vd
Pin DCL = 0dBm, Idq = 1.8A



IMD3 versus Pout & Temperature
Vd = 7V, Freq. = 7.5GHz



IMD3 versus Pout & Temperature
Vd = 6V, Freq. = 7.5GHz



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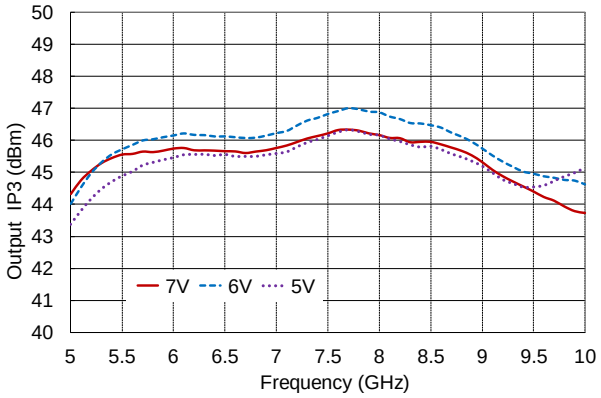
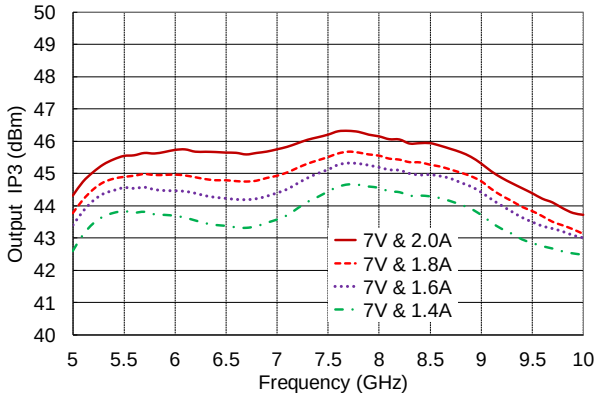
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Id = 1.8A

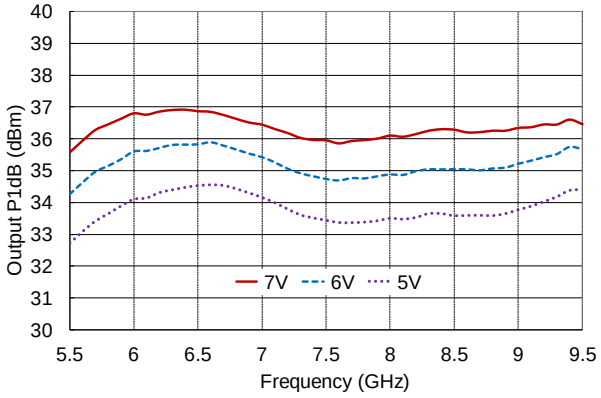
OIP3 versus Frequency & Vd
Idq = 2A, Pin DCL = 0dBm



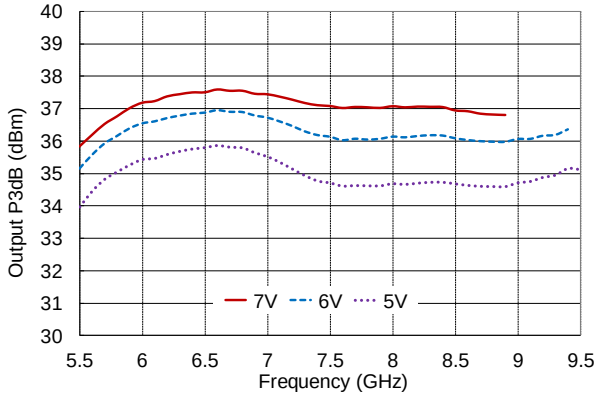
OIP3 versus Frequency & Current
Vd = 7V, Pin DCL = 0dBm



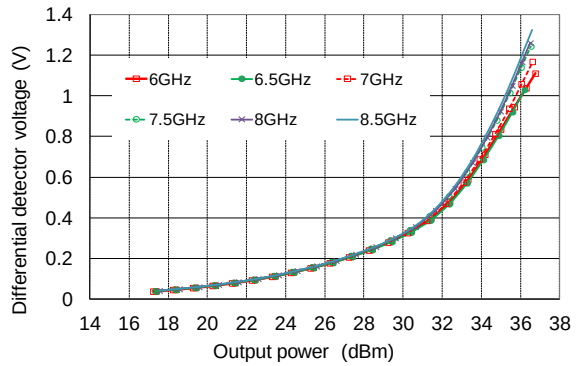
Pout at 1dB comp. vs Frequency & Vd
Idq = 2A



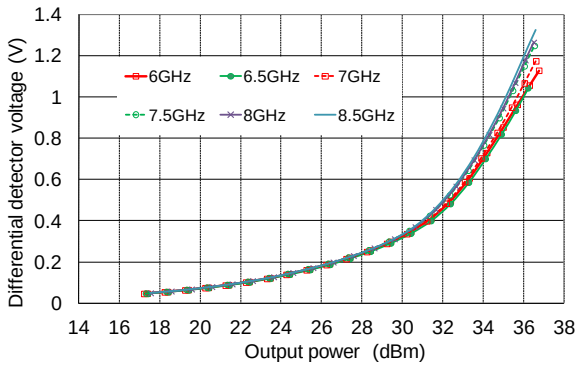
Pout at 3dB comp. vs Frequency & Vd
Idq = 2A



VREF1- VDET1 versus Pout
Vd = 7V



VREF2- VDET2 versus Pout
Vd = 7V



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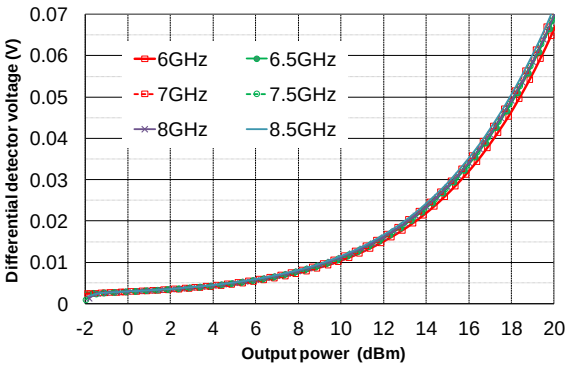
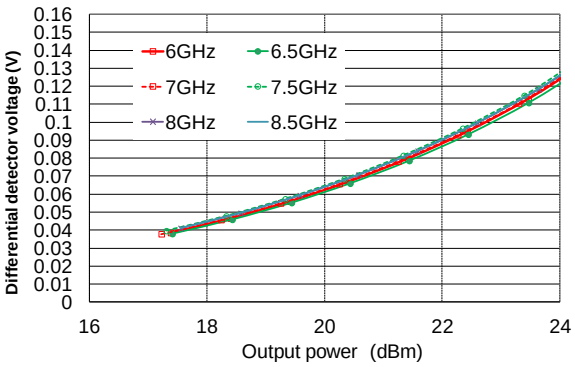
Typical Board Measurements

Tamb.= +25°C, Vd = +7.0V, Id = 1.8A

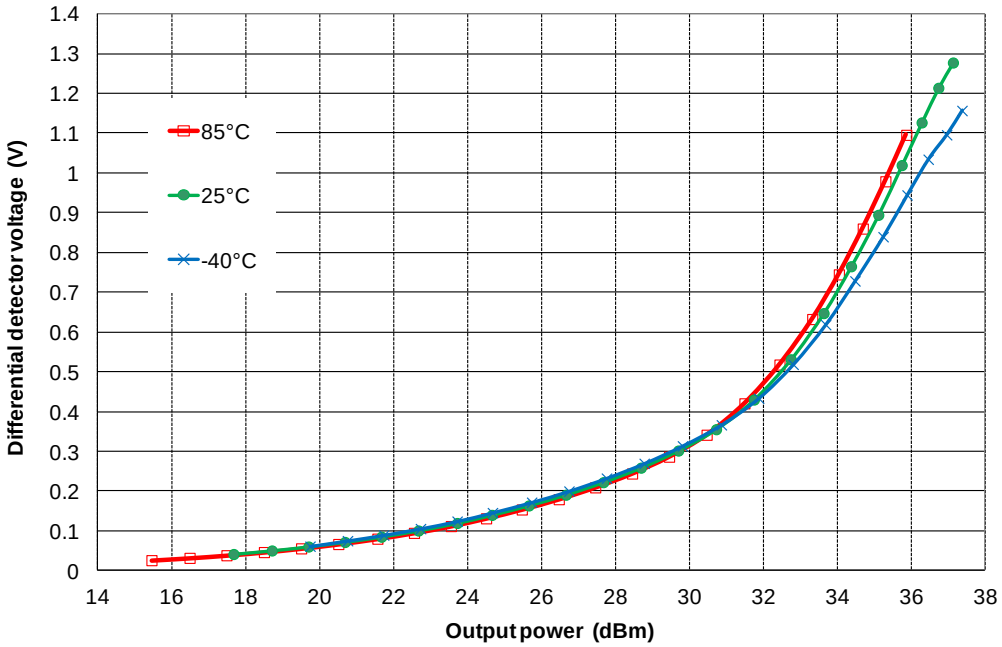
VREF1- VDET1 versus Pout
Vd = 7V & -2 < Pout < +20dBm



VREF1- VDET1 versus Pout
Vd = 7V & +18 < Pout < +24dBm



(VREF1-VDET1) versus Output Power & Temperature
Vd = 7V, Freq. = 7.5GHz & +16 < Pout < +36dBm



Please see paragraph “Notes” for more detail on detector

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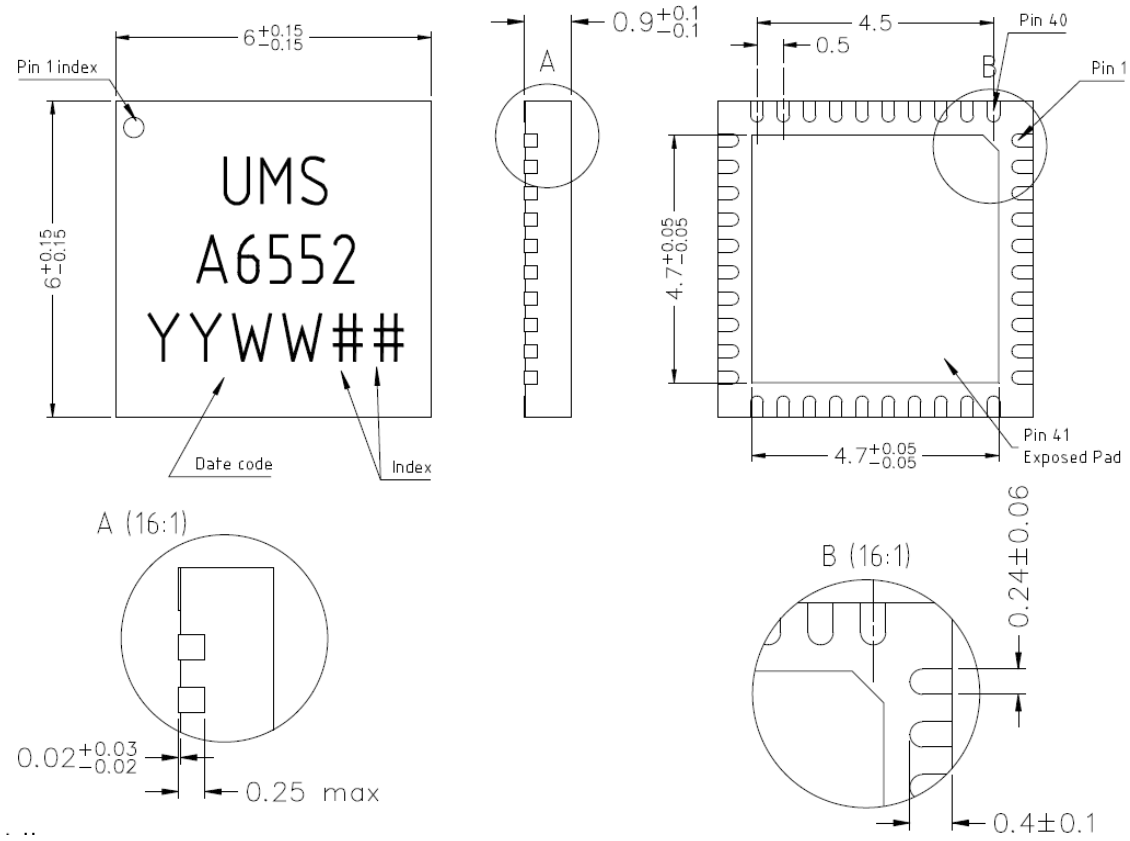
Package outline (1)



Matt tin, Lead Free	(Green)	1- Nc	15- Nc	29- VDC2
Units :	mm	2- Nc	16- VD2	30- VREF2
From the standard :	JEDEC MO-220 (VGGD)	3- Gnd(2)	17- VG2	31- Nc
		4- Gnd(2)	18- Nc	32- VD3
41-	GND	5- RF IN	19- VD3	33- Nc
		6- Gnd(2)	20- Nc	34- VG2
		7- Gnd(2)	21- Nc	35- VD2
		8- Nc	22- VREF1	36- Nc
		9- Nc	23- VDC1	37- VG1
		10- Nc	24- VDET1	38- VD1
		11- Nc	25- Gnd(2)	39- Gnd(2)
		12- Gnd(2)	26- RF OUT	40- Nc
		13- VD1	27- Gnd(2)	
		14- VG1	28- VDET2	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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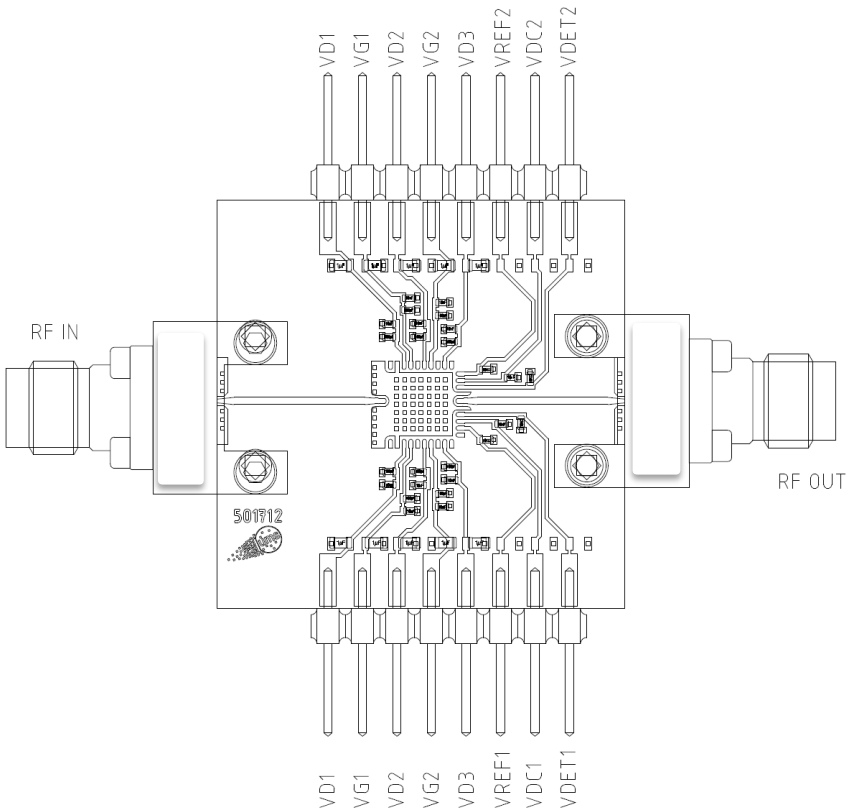
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for all DC accesses.
- A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



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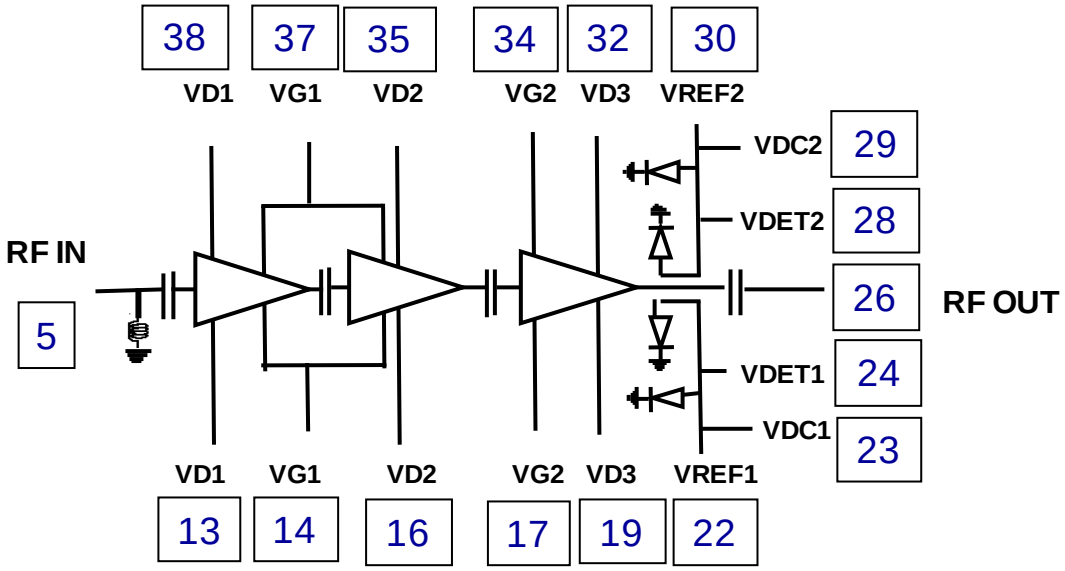
Notes

Due to ESD protection circuits on RF input, an external capacitance might be requested to isolate the product from the external voltage that could be present on the RF access.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 10nF, 1µF) on the PC board, as close as possible to the package.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.
Please note that it is not mandatory to use both detectors, on north and south sides.
If only one detector is used, the unused pads VDET, VREF and VDC could be unconnected or grounded.

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte Sn
MSL Rating	MSL3

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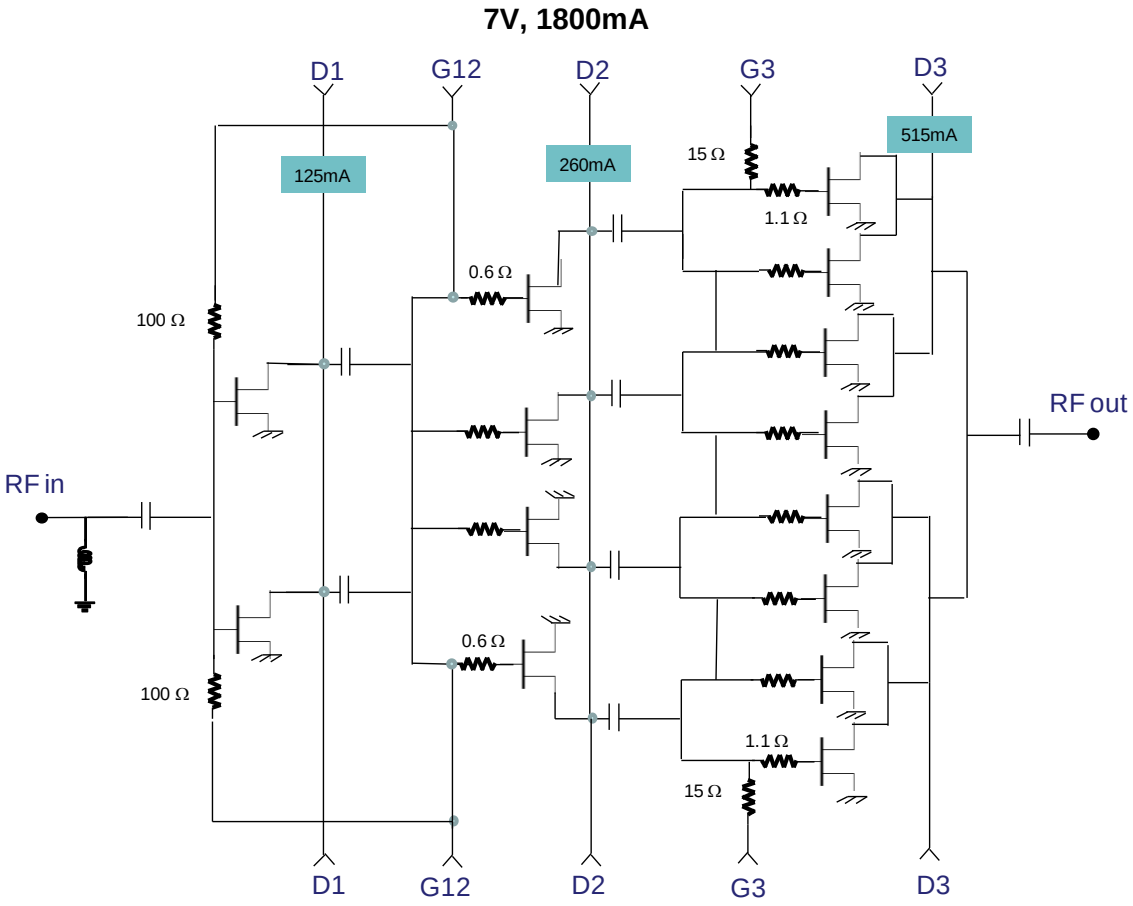
DC Schematic



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 6x6 package:	CHA6552-QJG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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