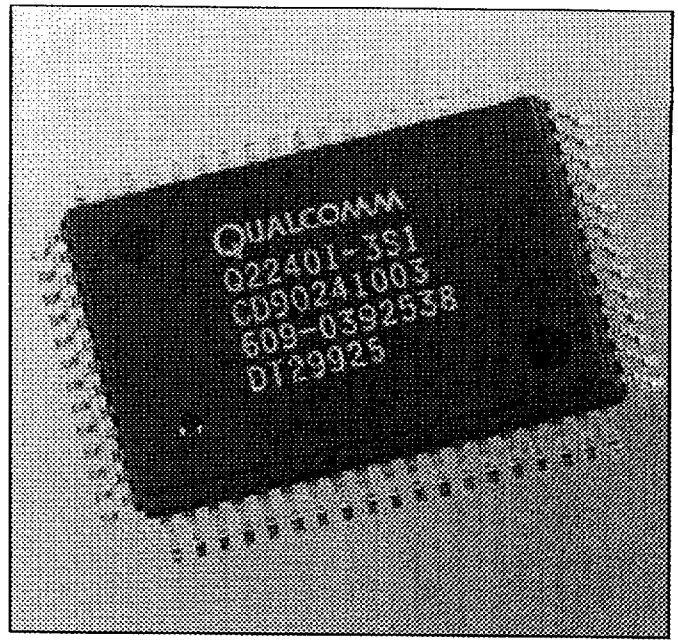
Q2240

DIRECT DIGITAL SYNTHESIZER



FEATURES

- Operation @ 5V or 3.3 V Supply
- 100 MHz Operation @ 5 V
- 60 MHz Operation @ 3.3 V
- 32-bit Input Resolution for Frequency
- 12-bit Output Resolution for Sine Wave Amplitude
- 14-bit Output Phase Resolution for Arbitrary Waveform Synthesis
- Q2240I-1N: Backwards Compatible with the Q2220I-50N
- Q2240I-2S1: Serial Control Interface
- Q2240I-3S1: 32-bit Direct Parallel Control Interface
- Q2240I-2S1: 14 x 20 mm, 64-pin PQFP
- Q2240I-3S1: 14 x 20 mm, 64-pin PQFP
- 100 MHz Frequency Update (Hop) Rate
- Arbitrary Waveform Mode
- Power-down Mode
- 3 Output Signal Formats: Offset Binary, 2's Complement, Sign Magnitude
- Guaranteed Over Industrial Temperature and Voltage Range

APPLICATIONS

- Digital Radios and Modems
- PC-based Instrumentation Cards
- Handheld Test and Measurement Equipment
- Portable Communications Terminals
- Digital Signal Processors
- Specialized Mobile Radios (SMR)
- Digital Video/Audio Signal Generation
- Arbitrary Waveform or Function Generator
- Baseband Transmitters and Receivers
- Mobile/Airborne Communications
- Frequency Hopping Systems
- Local Oscillator Generation
- Cellular Base Stations
- Spread Spectrum Modulators
- HF Transceivers
- Paging Systems

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Q2240 GENERAL DESCRIPTION

The Q2240 is a unique product family of Direct Digital Synthesizers (DDSs) that are ideally suited for the varied demands of digital wireless communications and complex waveform synthesis. Using CMOS technology, the Q2240 DDS series consists of three different package versions: Q2240I-1N, Q2240I-2S1, and the Q2240I-3S1. The Q2240I-1N is specified for operation with a +5 V power supply only, and is backwards compatible with the Q2220I-50N as a replaceable part. The Q2240I-2S1 and Q2240I-3S1, however, are specified for operation with a +5 V or +3.3 V power supply. The product family is described in the abbreviated feature set listed below for each version and summarized in Table 1.

MAXIMUM CLOCK SPEED

- 50 MHz for Q2240I-1N
- 100 MHz @ +5 V Supply for Q2240I-2S1 and -3S1
- 60 MHz @ +3.3 V Supply for Q2240I-2S1 and -3S1

DIGITAL INPUT/OUTPUT RESOLUTION

- 24-bit Input Frequency Resolution for Q2240I-1N
- 32-bit Input Frequency Resolution for Q2240I-2S1 and -3S1
- 10-bit Output Resolution for Q2240I-1N
- 12-bit Output Resolution for Q2240I-2S1 and -3S1
- 14-bit Output Phase Resolution for Q2240I-2S1 and -3S1

CONTROL INTERFACE

- 24-bit Direct Parallel Control for Q2240I-1N
- 32-bit Serial Control for Q2240I-2S1
- 32-bit Direct Parallel Control for Q2240I-3S1

FEATURE SET DISTINCTIONS

- Q2240I-1N: Backwards Compatible with Q2220I-50N DDS
- Q2240I-2S1 & -3S1: Arbitrary Waveform Mode and Power-down Mode

MAXIMUM FREQUENCY UPDATE RATE

- 50 MHz for Q2240I-1N
- 3 MHz for Q2240I-2S1
- 100 MHz for Q2240I-3S1

OUTPUT SIGNAL FORMATS

- Offset Binary & 2's Complement for Q2240I-1N
- Offset Binary, 2's Complement, & Sign Magnitude for Q2240I-2S1 and -3S1

Table 1. Q2240 Series Comparison

Parameter	Q2240I-1N	Q2240I-2S1	Q2240I-3S1
Maximum Clock	50 MHz	100 MHz	100 MHz
Input Resolution	24-bit	32-bit	32-bit
Output Resolution	10-bit	12-bit 14-bit (ϕ)	12-bit 14-bit (ϕ)
Control Interface	Direct Parallel	Serial	Direct Parallel
Frequency Update Rate	50 MHz	3 MHz	100 MHz
Feature Set	Q2220 Compatible	Power-down Arbitrary Waveform Mode 3 Output Formats	Power-down Arbitrary Waveform Mode 3 Output Formats
Supply Voltage	5V	3.3 V/ 5 V	3.3 V/ 5 V
Operating Temperature	-40 to 85°C	-40 to 85°C	-40 to 85°C
Package Style	44-pin PLCC	64-pin PQFP	64-pin PQFP

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BLOCK ARCHITECTURE

The basic block architecture for all three versions of the Q2240 DDS are shown in Figures 1-3. Functional distinctions will be identified in the subsequent sections. The input Frequency Control (FC) value is loaded into the DDS through either the serial interface or the parallel interface, depending on the respective version. The latched FC value is then accumulated in the phase accumulator at each system clock cycle. The accumulated phase value is passed to the sine look-up table (LUT) to give a sine amplitude value. The output of the LUT is put into a user-selected output format where it is then sent to the parallel outputs. All internal circuitry can be cleared by enabling the DDS reset function. For the Q2240I-2S1 and -3S1, the LUT can be bypassed by activating the Arbitrary Waveform Mode which sends the 14 MSBs out of the phase accumulator directly to the parallel outputs. The -2S1 and -3S1 versions are set for operation at either +3.3 V or +5 V supply voltage via the 3/5 SELECT input and can also be put into a Standby Power Mode by enabling the power-down function. These functional components are detailed in the following paragraphs for all three Q2240 versions.

DIGITAL PROCESSOR INTERFACE (DPI)

DIRECT PARALLEL INTERFACE

The Q2240I-1N and -3S1 are the direct parallel interface versions. All inputs to the frequency control register are available externally except the most significant bit (MSB). Internally, the MSB to the phase accumulator is set to "0". This coincides with the least significant 23 bits and 31 bits for the -1N version and -3S1 version being available as external inputs (i.e., FC[22:0] and FC[30:0] respectively). For fixed frequency applications (no tuning involved), processor control is not required since the external frequency control inputs can be hardwired. Each version supports both synchronous and asynchronous loading of the FC value. The method of loading is determined by the setting of the FCSELECT signal.

Asynchronous loading of the input frequency value is enabled when FCSELECT is set to a logic "High". In this case, the FC value is loaded into the FC Register at the rising edge of the input signal HOP CLK which can be completely asynchronous to the system clock. Internally, the HOP CLK signal is resynchronized to the SYS CLK signal which allows any frequency changes to be phase continuous.

Figure 1. Q2240I-1N Functional Block Diagram

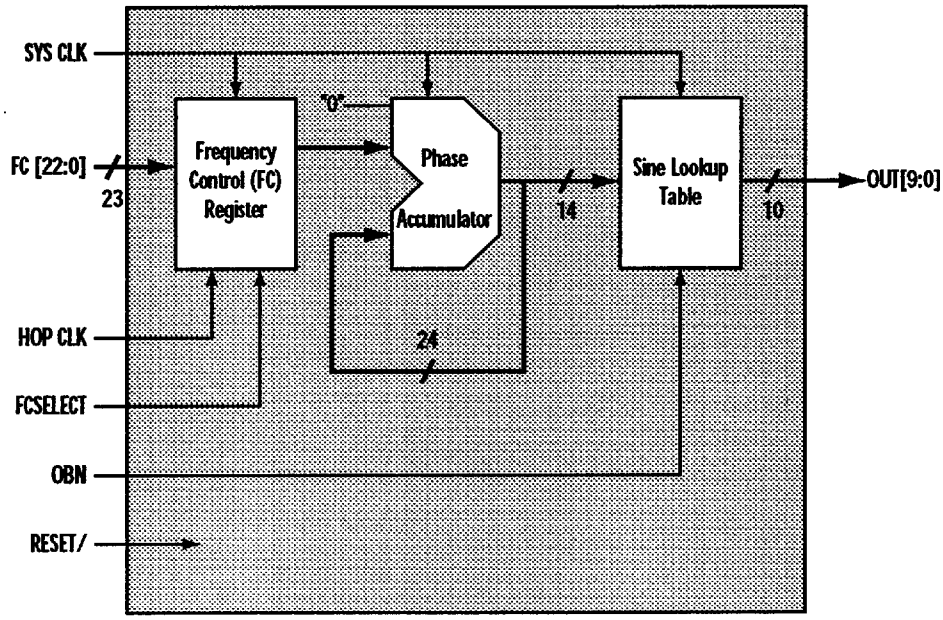

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Figure 2. Q2240I-2S1 Functional Block Diagram

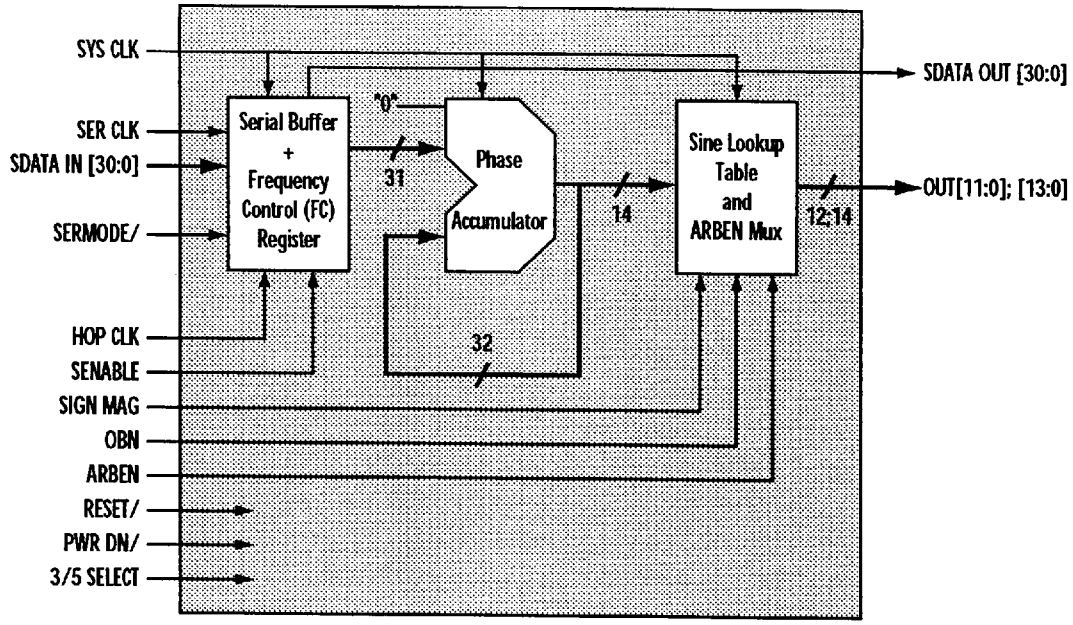
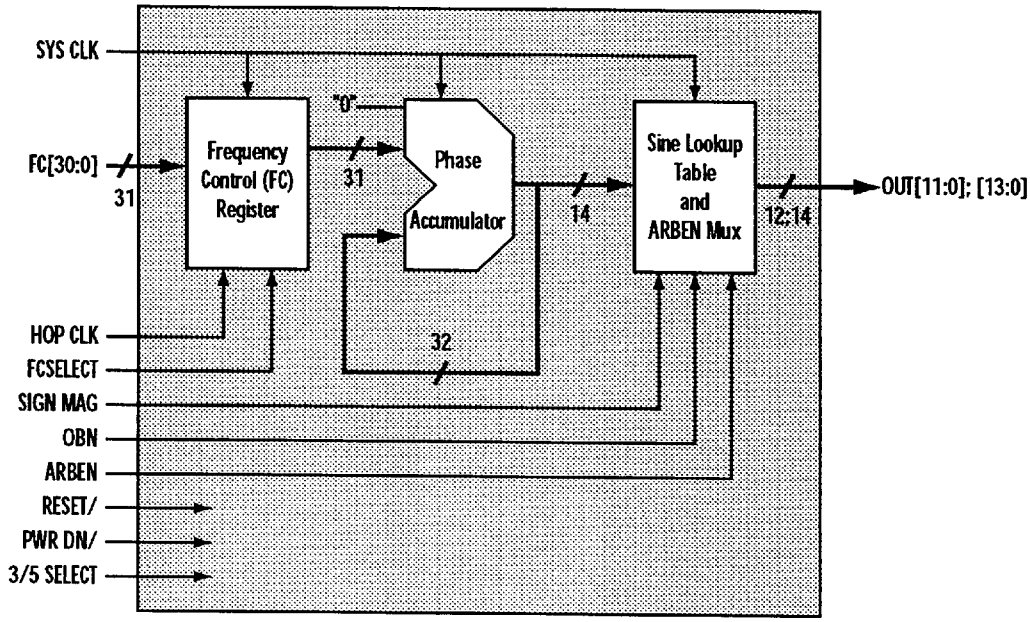


Figure 3. Q2240I-3S1 Functional Block Diagram



Alternatively, synchronous loading of the input frequency value is enabled when FCSELECT is set to a logic "Low". In this case, the FC value is loaded into the FC Register at the rising edge of each system clock signal SYS CLK. Using synchronous loading of the parallel inputs allows frequency changes as fast as the system clock frequency.

The loaded FC value will be completely cleared to zero when the input signal RESET/ is enabled. With the Q2240I-3S1, when the Power-down Mode is enabled the parallel interface is disabled and no new FC value can be loaded into the FC registers.

Note that prior to loading the FC value after supply voltage is first applied, the output of the DDS will

come up in a random state unless the RESET/ signal has been pulsed "Low". In this case, the output will be all zeros until the FC Register is loaded.

SERIAL INTERFACE

Serial control of the Q2240I-2S1 is accomplished in a standard fashion using four signals for loading in the FC value: SDATA IN, SER CLK, SENABLE, and HOP CLK. Note that first the input signal SERMODE/ must be set "Low" to enable the serial interface. (SERMODE/ is a static signal and asynchronous to any clock input.) With the SERMODE/ input set "Low", data is shifted serially bit by bit into SDATA IN on the rising edge of the SER CLK input while the shift enable control input, SENABLE, is set "High". To insure the timing integrity of the serial programming bits, it is necessary that the rising edge of the SER CLK signal does not exceed a 10% - 90% rise time of 15 nanoseconds. The serial programming sequence for the FC value consists of 31 bits in the order of MSB followed by LSB. As with the Q2240I-1N and -3S1 versions, internally the highest MSB (bit 32) to the phase accumulator is set to "0". The loaded FC value is stored in the 31-bit serial buffer registers clocked by the SER CLK signal. The SENABLE input must be held "High" for the entire serial programming sequence and then set "Low". Letting the SENABLE go "Low" before all of the serial programming bits are loaded into the serial registers will result in erroneous programming to the serial registers. After the SENABLE input is set "Low", the serial register contents are activated on the rising edge of the HOP CLK input according to the timing requirements shown in Figure 13 and Table 22. A serial data output, SDATA OUT, is provided to facilitate daisy-chaining to another Q2240I-2S1 or other serial-controlled devices. This means that at the same time when the 31-bit FC value is being serially shifted into the serial buffer registers, the last 31-bit FC value stored in the buffer is being shifted out of the DDS through the SDATA OUT with MSB leading LSB.

The loaded FC value will be completely cleared to zero when the input signal RESET/ is enabled. Additionally, when the Power-down Mode is enabled, the serial interface which runs on SER CLK is not disabled. This means that even during a power-down condition, an FC value can still be serially shifted into the serial buffer registers. In this case when the DDS is activated to a power-up condition, the FC value can then be loaded into the FC Register by asserting the HOP CLK signal. Note that prior to loading the FC value after supply voltage is first applied, the output of the DDS will come up in a random state unless the RESET/ signal has been pulsed "Low". In this case, the output will be all zeros until the FC Register is loaded.

ARBITRARY WAVEFORM MODE

In addition to standard sine wave generation, the Q2240I-2S1 and -3S1 are designed to provide a sine lookup bypass function which will output the upper bits of the phase accumulator directly instead of being mapped into and through the sine LUT. This allows the Q2240 to form the basis of an arbitrary waveform generator. When used in this mode, general waveform mapping can be accomplished using an external RAM or RAMDAC that is loaded with the desired sampled signal. The Arbitrary Waveform Mode is enabled when the ARBEN input is set to a logic "High". When activated, this function will direct the 14 MSB output bits of the phase accumulator directly as the DDS digital outputs (OUT0 - OUT 13). In this case, the unused sine LUT is deactivated internally to reduce the overall Q2240 current consumption, as seen in the comparative measurements shown in Figures 4 and 5. All DDS control functions remain equally valid during operation for standard sine wave generation or in Arbitrary Waveform Mode with the exception that the output format selection does not apply since the binary coding options are only for the sine amplitude output. Output pins OUT12 and OUT13 are dedicated output signals used in Arbitrary Waveform Mode only and remain inactive to reduce switching noise when this mode is disabled by setting the ARBEN input to "Low".

POWER-DOWN MODE

The Q2240I-2S1 and -3S1 provide a Power-down Mode to minimize power consumption when the DDS is not in use. The Power-down Mode is enabled when the input signal PWR DN/ is set to a logic "Low". The

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Figure 4. Q2240 Typical Current Consumption vs. Frequency at V_{DD} = 5 V
("Worst Case" test pattern was used to obtain the above measurements, FC data = Hex 77787777.)

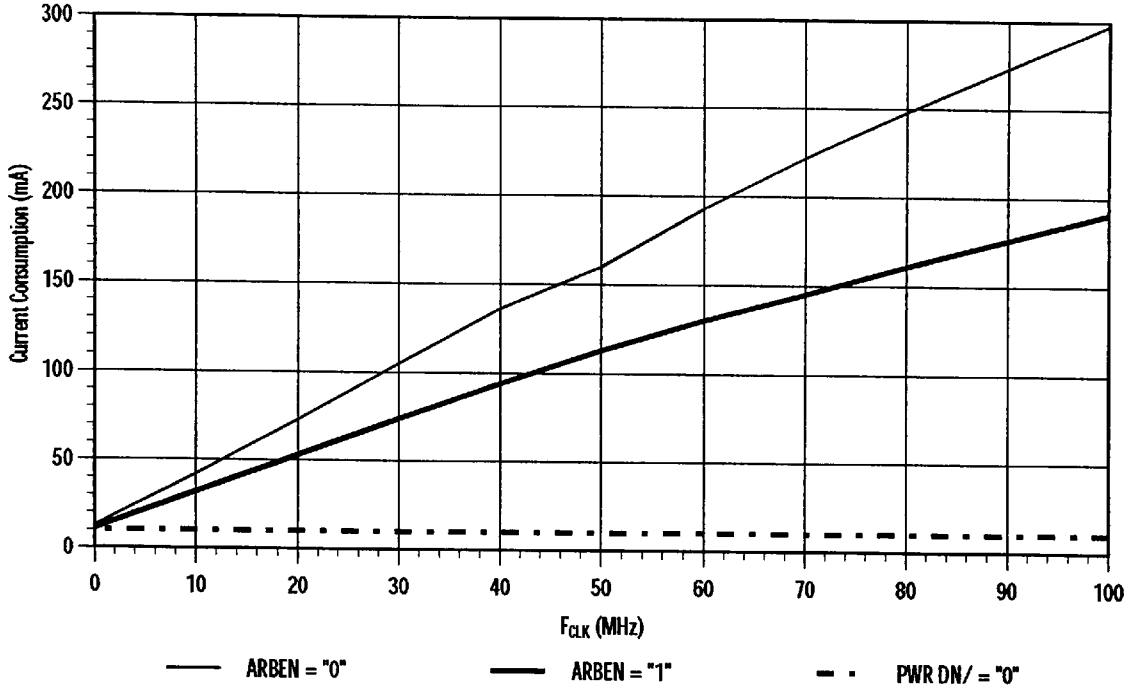
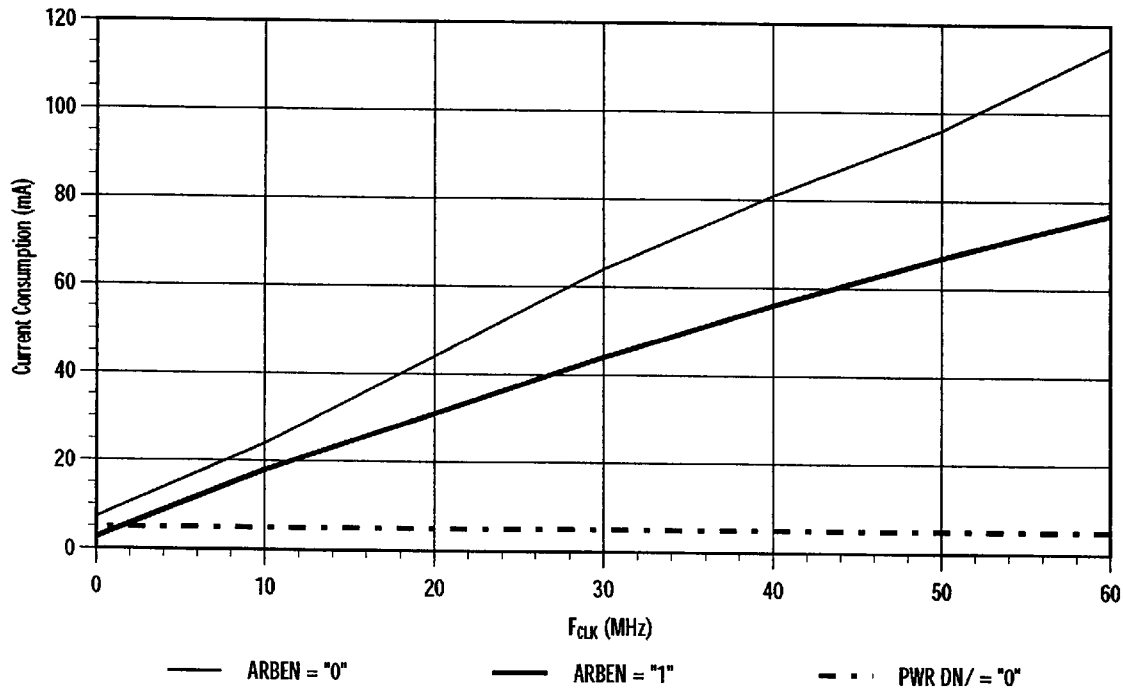


Figure 5. Q2240 Typical Current Consumption vs. Frequency at V_{DD} = 3.3 V
("Worst Case" test pattern was used to obtain the above measurements, FC data = Hex 77787777.)



PWR DN/ control is a static signal and asynchronous to any clock input. The DDS is kept in a power-down condition as long as PWR DN/ is enabled causing current consumption to be reduced to within 10 mA or less (see Figures 4 and 5 for typical current consumption measurements). Internally, the PWR DN/ signal is synchronized to the input signal SYS CLK to guarantee there will be phase continuity going into and coming out of Power-down Mode. When power-down is activated, all internal registers will retain their values prior to power-down and the active digitized output value will freeze at the DDS outputs. This means that when power-down is disabled and the DDS is activated to a power-up condition, previous phase continuity will be maintained, even with the given latency effect to the DDS outputs. Additionally, the reset function (RESET/) can be used while in Power-down Mode, if desired.

RESET

A reset function is provided for all Q2240 versions to allow all output signals and internal registers to be cleared. Reset is enabled when the input signal RESET/ is set to a logic "Low". The RESET/ control is a static signal and asynchronous to any clock input. The RESET/ should not be left in a floating condition. If unused, connect the RESET/ signal to a "High" setting through a pull-up resistor to V_{DD} to ensure that the device does not hang in a reset state (typical pull-up resistor values are between 5 kΩ to 20 kΩ). When the reset function is activated, the FC Register, Serial Buffer, Phase Accumulator, Sine LUT, and Output are set to "0". The DDS output will remain at the reset level until RESET/ is disabled by setting to a logic "High". When RESET/ is disabled, the Q2240 can be loaded with a new FC value immediately and the accumulation process will begin again. The DDS output will be at "0" until valid outputs are available at the output registers after a fixed latency (see *Timing Specifications*section).

OUTPUT FORMAT

For the Q2240I-1N, output format selection of the sine amplitude output is provided to support either Offset Binary or Offset Two's Complement binary coding. The amplitude output is formatted using Offset Binary notation when the input signal OBN is set to a logic "High". When OBN is set "Low", the output format is Offset Two's Complement.

For the Q2240I-2S1 and -3S1, output format selection of the sine amplitude output is provided to support either Offset Binary, Offset Sign Magnitude, or Offset Two's Complement binary coding. The output format is selected depending on the settings of the input signals OBN and SIGN MAG as follows:

OBN = "High", SIGN MAG = "Low" :
Selects Offset Binary

OBN = "Low", SIGN MAG = "High" :
Selects Offset Sign Magnitude

OBN = "Low", SIGN MAG = "Low" :
Selects Offset Two's Complement

OBN = "High", SIGN MAG = "High" :
Selects Offset Two's Complement

Table 2 shows the effect of the output format for output signals OUT [11:0].

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Table 2. Q2240 Output Formats

OUTPUT VALUE	OFFSET BINARY MSB LSB	SIGN MAGNITUDE MSB LSB	TWO's COMPLEMENT MSB LSB
MAX Value	111111111111	011111111111	011111111111
...	111111111110	011111111110	011111111110
...	...	...	...
...	...	...	...
Half MAX + 1	100000000000	000000000000	000000000000
Half MAX – 1	011111111111	100000000000	111111111111
...	...	...	...
...	...	...	...
...	000000000001	111111111110	100000000001
MIN Value	000000000000	111111111111	100000000000

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INPUT/OUTPUT PIN FUNCTIONS

There are three different versions of the Q2240 DDS. The Q2240I-1N is backwards compatible with the Q2220I-50N and is controlled via a parallel interface, the Q2240I-2S1 is controlled via a serial interface, and the Q2240I-3S1 is controlled via a parallel interface. All three versions have unique I/O pin functions. Figure 6 and Tables 3-6 show the pinout diagram and I/O pin function tables for the Q2240I-1N (24-bit parallel interface, Q2220I-50N replacement). Figure 7 and Tables 7-9 show the pinout diagram and I/O pin function tables for the Q2240I-2S1 (serial interface). Figure 8 and Tables 10-13 show the pinout diagram and I/O pin function tables for the Q2240I-3S1 (32-bit parallel interface).

Figure 6. Q2240I-1N (24-bit Parallel Interface) Pinout Diagram

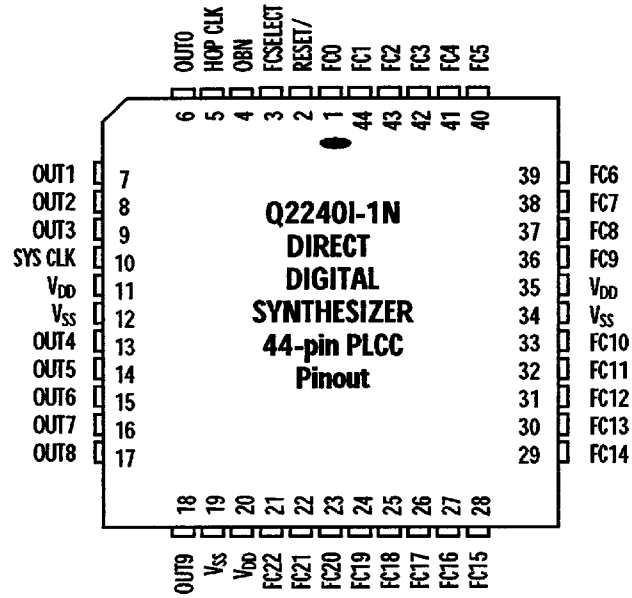

Table 3. Q2240I-1N (24-bit Parallel Interface) Control/Input Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
SYS CLK	10	TTL INPUT	System Clock.
RESET/	2	TTL INPUT	Reset Enable. (Active "Low"), clears FC register, phase accumulator, sine LUT and output.
FCSELECT	3	TTL INPUT	Selects which clock activates the FC value (0=SYS CLK, 1= HOP CLK).
OBN	4	TTL INPUT	Offset Binary Format Select. When "High", sets the output to be in offset binary format (internal 25 k pull-down). Output to be in 2's Complement when set "Low".
HOP CLK	5	TTL INPUT	Asynchronous Load Signal (internal 25 k pull-up), Input FC Value is activated on rising edge of HOP CLK if FCSELECT is set "High".

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Table 4. Q2240I-1N (24-bit Parallel Interface) Frequency Control Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
FC0	1	TTL INPUT	Frequency Control Bit 0 (LSB) (Internal 25 k Pull-up)
FC1	44	TTL INPUT	Frequency Control Bit 1 (Internal 25 k Pull-up)
FC2	43	TTL INPUT	Frequency Control Bit 2 (Internal 25 k Pull-up)
FC3	42	TTL INPUT	Frequency Control Bit 3 (Internal 25 k Pull-up)
FC4	41	TTL INPUT	Frequency Control Bit 4 (Internal 25 k Pull-up)
FC5	40	TTL INPUT	Frequency Control Bit 5 (Internal 25 k Pull-up)
FC6	39	TTL INPUT	Frequency Control Bit 6 (Internal 25 k Pull-up)
FC7	38	TTL INPUT	Frequency Control Bit 7 (Internal 25 k Pull-up)
FC8	37	TTL INPUT	Frequency Control Bit 8 (Internal 25 k Pull-up)
FC9	36	TTL INPUT	Frequency Control Bit 9 (Internal 25 k Pull-up)
FC10	33	TTL INPUT	Frequency Control Bit 10 (Internal 25 k Pull-up)
FC11	32	TTL INPUT	Frequency Control Bit 11 (Internal 25 k Pull-up)
FC12	31	TTL INPUT	Frequency Control Bit 12 (Internal 25 k Pull-up)
FC13	30	TTL INPUT	Frequency Control Bit 13 (Internal 25 k Pull-up)
FC14	29	TTL INPUT	Frequency Control Bit 14 (Internal 25 k Pull-up)
FC15	28	TTL INPUT	Frequency Control Bit 15 (Internal 25 k Pull-up)
FC16	27	TTL INPUT	Frequency Control Bit 16 (Internal 25 k Pull-up)
FC17	26	TTL INPUT	Frequency Control Bit 17 (Internal 25 k Pull-up)
FC18	25	TTL INPUT	Frequency Control Bit 18 (Internal 25 k Pull-up)
FC19	24	TTL INPUT	Frequency Control Bit 19 (Internal 25 k Pull-up)
FC20	23	TTL INPUT	Frequency Control Bit 20 (Internal 25 k Pull-up)
FC21	22	TTL INPUT	Frequency Control Bit 21 (Internal 25 k Pull-up)
FC22	21	TTL INPUT	Frequency Control Bit 22 (Internal 25 k Pull-up)

Table 5. Q2240I-1N (24-bit Parallel Interface) Data Output Pin Functions

SYMBOL	PINS	I/O TYPE*	NAME AND FUNCTION
OUT0	6	CMOS OUTPUT	Data OUTPUT Bit 0 (LSB)
OUT1	7	CMOS OUTPUT	Data OUTPUT Bit 1
OUT2	8	CMOS OUTPUT	Data OUTPUT Bit 2
OUT3	9	CMOS OUTPUT	Data OUTPUT Bit 3
OUT4	13	CMOS OUTPUT	Data OUTPUT Bit 4
OUT5	14	CMOS OUTPUT	Data OUTPUT Bit 5
OUT6	15	CMOS OUTPUT	Data OUTPUT Bit 6
OUT7	16	CMOS OUTPUT	Data OUTPUT Bit 7
OUT8	17	CMOS OUTPUT	Data OUTPUT Bit 8
OUT9	18	CMOS OUTPUT	Data OUTPUT Bit 9

*±8 mA drive strength at V_{DD} = 5.0 V (± 10%).

Table 6. Q2240I-1N (24-bit Parallel Interface) Voltage Supply Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
V_{DD}	11, 20, 35	PWR	Power (+ 5 VDC)
V_{SS}	12, 19, 34	GND	Ground

Figure 7. Q2240I-2S1 (Serial Interface) Pinout Diagram

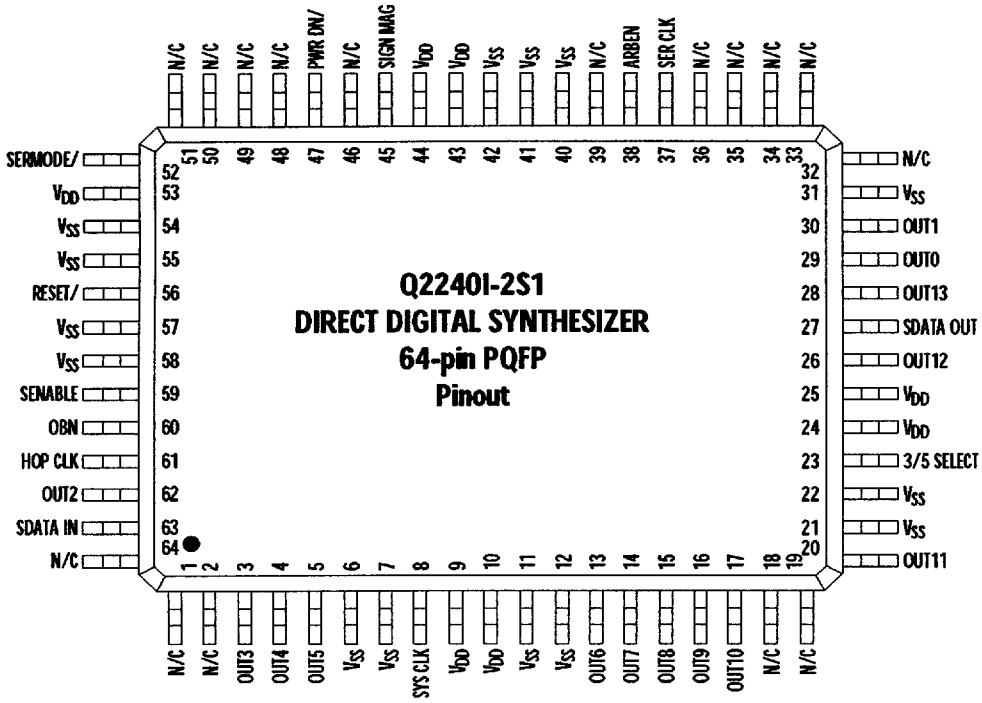

Table 7. Q2240I-2S1 (Serial Interface) Control/Input Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
SYS CLK	8	TTL INPUT	System Clock.
3/5 SELECT	23	CMOS INPUT	Tied to "Low" for 5 V operation, "High" for 3.3 V operation (internal 40 k pull-down).
SER CLK	37	TTL INPUT	Serial Data Clock (internal 25 k pull-up). Shifts serial data into SDATA IN with each rising edge.
ARBEN	38	TTL INPUT	Arbitrary Waveform Enable (Active "High"), enables the DDS to directly output the 14 MSB's of the phase accumulator (internal 25 k pull-down).
SIGN MAG	45	TTL INPUT	Sign Magnitude (Active "High"), sets the output to be in Sign Magnitude format (internal 25 k pull-down).
PWR DN/	47	TTL INPUT	Power-down Enable (Active "Low"), (internal 25 k pull-up).
SERMODE/	52	TTL INPUT	Serial Mode Enable (Active "Low"). Enables the Serial Data Interface. (Internal 25 k pull-up)
RESET/	56	TTL INPUT	Reset Enable. (Active "Low"), clears FC register, phase accumulator, sine LUT and output.
SENABLE	59	TTL INPUT	Serial Shift Enable (Active "High"), for loading input serial data, SDATA IN.
OBN	60	TTL INPUT	Offset Binary Format Select. (Active "High"), sets the output to be in Offset Binary format (internal 25 k pull-down).
HOP CLK	61	TTL INPUT	Asynchronous Load Signal (internal 25 k pull-up). Input serial data is activated on rising edge of HOP CLK after SENABLE is set "Low".
SDATA IN	63	TTL INPUT	Serial Data Input (internal 25 k pull-up). Data is shifted in serially on rising edge of SER CLK.

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Table 8. Q2240I-2S1 (Serial Interface) Data Output Pin Functions

SYMBOL	PINS	I/O TYPE*	NAME AND FUNCTION
OUT0	29	CMOS OUTPUT	Data OUTPUT Bit 0 (LSB)
OUT1	30	CMOS OUTPUT	Data OUTPUT Bit 1
OUT2	62	CMOS OUTPUT	Data OUTPUT Bit 2
OUT3	3	CMOS OUTPUT	Data OUTPUT Bit 3
OUT4	4	CMOS OUTPUT	Data OUTPUT Bit 4
OUT5	5	CMOS OUTPUT	Data OUTPUT Bit 5
OUT6	13	CMOS OUTPUT	Data OUTPUT Bit 6
OUT7	14	CMOS OUTPUT	Data OUTPUT Bit 7
OUT8	15	CMOS OUTPUT	Data OUTPUT Bit 8
OUT9	16	CMOS OUTPUT	Data OUTPUT Bit 9
OUT10	17	CMOS OUTPUT	Data OUTPUT Bit 10
OUT11	20	CMOS OUTPUT	Data OUTPUT Bit 11 (MSB for Sine Wave Output)
OUT12	26	CMOS OUTPUT	Data OUTPUT Bit 12
OUT13	28	CMOS OUTPUT	Data OUTPUT Bit 13 (MSB for Arbitrary Waveform Mode)
SDATA OUT	27	CMOS OUTPUT	Serial Data OUTPUT; Used for Daisy-chaining Serial Controlled Devices

*$\pm$8 mA drive strength at V_{DD} = 5.0 V ($\pm$ 10%). Derated to $\pm$ 7 mA drive strength for 3.3 V operation.

Table 9. Q2240I-2S1 (Serial Interface) Voltage Supply Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
V_{DD}	9, 10, 24, 25, 43, 44, 53	PWR	Power (3.3 V or 5 V Depending on Input 3/5 SELECT State)
V_{SS}	6, 7, 11, 12, 21, 22, 31, 40, 41, 42, 54, 55, 57, 58	GND	Ground
N/C	1, 2, 18, 19, 32, 33, 34, 35, 36, 39, 46, 48, 49, 50, 51	NO CONNECT	Unconnected Pin

Figure 8. Q2240I-3S1 (32-bit Parallel Interface) Pinout Diagram

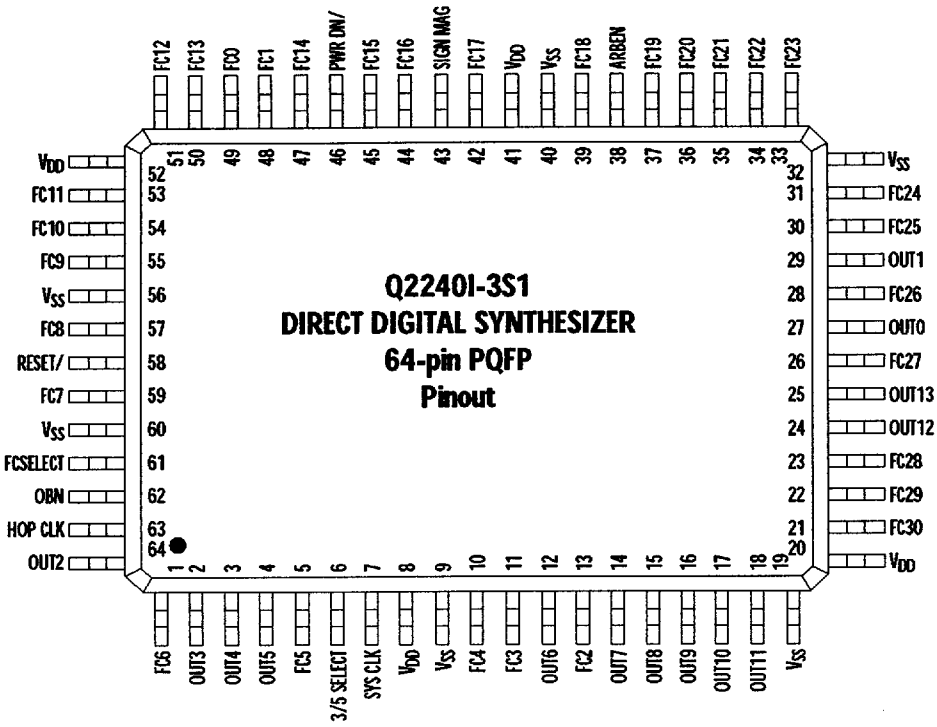

Table 10. Q2240I-3S1 (32-bit Interface) Control/Input Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
3/5 SELECT	6	CMOS INPUT	Tied to "Low" for 5 V operation, "High" for 3.3 V operation (internal 40 k pull-down).
SYS CLK	7	TTL INPUT	System Clock.
ARBEN	38	TTL INPUT	Arbitrary Waveform Enable (Active "High"), enables the DDS to directly output the 14 MSB's of the phase accumulator (internal 25 k pull-down).
SIGN MAG	43	TTL INPUT	Sign Magnitude (Active "High"), sets the output to be in Sign Magnitude format (internal 25 k pull-down).
PWR DN/	46	TTL INPUT	Power Down Enable (Active "Low"), (internal 25 k pull-up).
RESET/	58	TTL INPUT	Reset Enable. (Active "Low"), clears FC register, phase accumulator, sine LUT and output.
FCSELECT	61	TTL INPUT	Selects which clock activates the FC value (0=SYS CLK, 1= HOP CLK).
OBN	62	TTL INPUT	Offset Binary Format Select. When "High", sets the output to be in Offset Binary format (internal 25 k pull-down).
HOP CLK	63	TTL INPUT	Asynchronous Load Signal (internal 25 k pull-up), Input FC Value is activated on rising edge of HOP CLK if FCSELECT is set "High".

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Table 11. Q2240I-3S1 (32-bit Parallel Interface) Frequency Control Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
FC0	49	TTL INPUT	Frequency Control Bit 0 (LSB) (Internal 25 k Pull-down)
FC1	48	TTL INPUT	Frequency Control Bit 1 (Internal 25 k Pull-down)
FC2	13	TTL INPUT	Frequency Control Bit 2 (Internal 25 k Pull-down)
FC3	11	TTL INPUT	Frequency Control Bit 3 (Internal 25 k Pull-down)
FC4	10	TTL INPUT	Frequency Control Bit 4 (Internal 25 k Pull-down)
FC5	5	TTL INPUT	Frequency Control Bit 5 (Internal 25 k Pull-down)
FC6	1	TTL INPUT	Frequency Control Bit 6 (Internal 25 k Pull-down)
FC7	59	TTL INPUT	Frequency Control Bit 7 (Internal 25 k Pull-down)
FC8	57	TTL INPUT	Frequency Control Bit 8 (Internal 25 k Pull-up)
FC9	55	TTL INPUT	Frequency Control Bit 9 (Internal 25 k Pull-up)
FC10	54	TTL INPUT	Frequency Control Bit 10 (Internal 25 k Pull-up)
FC11	53	TTL INPUT	Frequency Control Bit 11 (Internal 25 k Pull-up)
FC12	51	TTL INPUT	Frequency Control Bit 12 (Internal 25 k Pull-up)
FC13	50	TTL INPUT	Frequency Control Bit 13 (Internal 25 k Pull-up)
FC14	47	TTL INPUT	Frequency Control Bit 14 (Internal 25 k Pull-up)
FC15	45	TTL INPUT	Frequency Control Bit 15 (Internal 25 k Pull-up)
FC16	44	TTL INPUT	Frequency Control Bit 16 (Internal 25 k Pull-up)
FC17	42	TTL INPUT	Frequency Control Bit 17 (Internal 25 k Pull-up)
FC18	39	TTL INPUT	Frequency Control Bit 18 (Internal 25 k Pull-up)
FC19	37	TTL INPUT	Frequency Control Bit 19 (Internal 25 k Pull-up)
FC20	36	TTL INPUT	Frequency Control Bit 20 (Internal 25 k Pull-up)
FC21	35	TTL INPUT	Frequency Control Bit 21 (Internal 25 k Pull-up)
FC22	34	TTL INPUT	Frequency Control Bit 22 (Internal 25 k Pull-up)
FC23	33	TTL INPUT	Frequency Control Bit 23 (Internal 25 k Pull-up)
FC24	31	TTL INPUT	Frequency Control Bit 24 (Internal 25 k Pull-up)
FC25	30	TTL INPUT	Frequency Control Bit 25 (Internal 25 k Pull-up)
FC26	28	TTL INPUT	Frequency Control Bit 26 (Internal 25 k Pull-up)
FC27	26	TTL INPUT	Frequency Control Bit 27 (Internal 25 k Pull-up)
FC28	23	TTL INPUT	Frequency Control Bit 28 (Internal 25 k Pull-up)
FC29	22	TTL INPUT	Frequency Control Bit 29 (Internal 25 k Pull-up)
FC30	21	TTL INPUT	Frequency Control Bit 30 (Internal 25 k Pull-up)

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Table 12. Q2240I-3S1 (32-bit Parallel Interface) Data Output Pin Functions

SYMBOL	PINS	I/O TYPE*	NAME AND FUNCTION
OUT0	27	CMOS OUTPUT	Data OUTPUT Bit 0 (LSB)
OUT1	29	CMOS OUTPUT	Data OUTPUT Bit 1
OUT2	64	CMOS OUTPUT	Data OUTPUT Bit 2
OUT3	2	CMOS OUTPUT	Data OUTPUT Bit 3
OUT4	3	CMOS OUTPUT	Data OUTPUT Bit 4
OUT5	4	CMOS OUTPUT	Data OUTPUT Bit 5
OUT6	12	CMOS OUTPUT	Data OUTPUT Bit 6
OUT7	14	CMOS OUTPUT	Data OUTPUT Bit 7
OUT8	15	CMOS OUTPUT	Data OUTPUT Bit 8
OUT9	16	CMOS OUTPUT	Data OUTPUT Bit 9
OUT10	17	CMOS OUTPUT	Data OUTPUT Bit 10
OUT11	18	CMOS OUTPUT	Data OUTPUT Bit 11 (MSB for Sine Wave Output)
OUT12	24	CMOS OUTPUT	Data OUTPUT Bit 12
OUT13	25	CMOS OUTPUT	Data OUTPUT Bit 13 (MSB for Arbitrary Waveform Mode)

*±8 mA drive strength at V_{DD} = 5.0 V (± 10%). Derated to ± 7 mA for 3.3 V operation.

Table 13. Q2240I-3S1 (32-bit Parallel Interface) Voltage Supply Pin Functions

SYMBOL	PINS	I/O TYPE	NAME AND FUNCTION
V_{DD}	8, 20, 41, 52	PWR	Power (3.3 or 5 V Depending on Input 3/5 SELECT State)
V_{SS}	9, 19, 32, 40, 56, 60	GND	Ground

THERMAL MANAGEMENT CONSIDERATIONS FOR THE Q2240I-2S1 AND Q2240I-3S1

DDS power consumption is directly proportional to the frequency of the applied clock reference. Figures 4 and 5 show typical current consumption vs. frequency over various operating conditions. Because of the relatively high power dissipation at the higher system clock frequencies, thermal management is a key design consideration. When applying a DDS clock frequency above 80 MHz, precautions should be taken at the very beginning of the design phase to ensure reliable operation of the DDS device under worse-case operating conditions. Although the PQFP package is qualified with a low junction-to-ambient thermal resistance (θ_{JA} = 32°C/W typical), operation in ambient environments approaching +85°C or above may require thermal enhancement techniques to sustain the junction temperature below the rated +150°C (see *Technical Specifications* section for reference). For operating environments below +85° C or lower system clock frequencies, the Q2240 does not require any special thermal management considerations. Some design suggestions to facilitate efficient thermal management when operating in severe ambient conditions at high clock frequencies are given below:

1. Attachable heat sinks to the PQFP package can be used to help lower the effective thermal resistance.
2. Forced convection airflow over the package surface may be appropriate in certain situations. Again, this has the effect of helping to lower the effective thermal resistance.
3. The printed circuit board (PCB) should have at least 4 layers, placing the power and/or ground plane close to the surface beneath the PQFP. Use as many vias as practical anywhere beneath the PQFP area connected to the power and/or ground planes.
4. The PCB should have 2 oz. copper (64 micron, 2.6 mil thick) or more instead of the standard 1 or 0.5 oz., at least in the PQFP area.
5. Solder all pins to the PCB (including unconnected pins). Additionally, wide PCB traces from the Q2240 pins can help to remove heat from the device.

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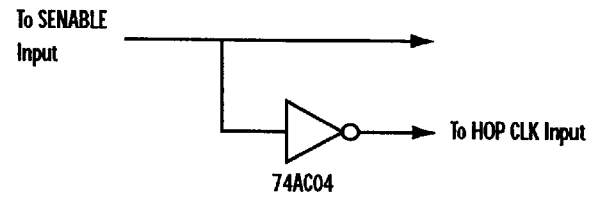
6. Thermally conductive, electrically isolated epoxy or other thermal interface material placed beneath the PQFP before reflow attach can significantly improve thermal coupling with the PCB.
7. Total thermal load from other components or materials in the area of the PQFP should be minimized.
8. Place the PQFP near a large thermal mass such as a PCB edge connector, for example. This has the effect of being an indirect heat sink mass for the dissipating power.
9. Thermal "Pillows" are available to be placed on hot components and conduct heat to other surfaces, such as a metal case.

USING 3-WIRE EQUIVALENT SERIAL CONTROL FOR THE Q2240I-2S1

Although serial control for the Q2240I-2S1 is accomplished using four signals (SDATA IN, SER CLK, SENABLE and HOP CLK), a 3-wire control method can be easily implemented with the addition of a simple CMOS Inverter as shown in Figure 9. Additional reference is found under *Digital Processor Interface* the *Serial Interface* section, and in the *Serial Interface Timing* information contained in Figure 13 and Table 22.

Figure 9. 3-wire Serial Control Implementation



TECHNICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 14 shows the absolute maximum ratings for all Q2240 versions. Table 15 shows the operating ranges of the Q2240I-1N, and Table 16 shows the operating ranges of the Q2240I-2S1 and Q2240I-3S1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damgage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 14. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	- 0.3	+ 7.0	V	–
Voltage on Any Input or Output Pin	–	- 0.3	V_{DD} + 0.3	V	–
Storage Temperature	T_S	- 55	+ 150	°C	–
Junction Temperature	T_J	–	+ 150	°C	–
I/O Electrostatic Discharge Protection	V_{ESD}	- 2000	+ 2000	V	1
I/O Latch-Up Trigger Current Protection	I_{TRIG}	- 150	+ 150	mA	1

Notes:

1. Test method meets the intent MIL-STD-883C Method 3015.

Table 15. Q2240I-1N Operating Range

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Temperature (Ambient)	T_A	- 40	–	+ 85	°C	–
Operating Supply Voltage	V_{DD}	4.5	–	5.5	V	–
Junction to Ambient Resistance	θ_{JA}	–	41	–	°C/W	1
Junction to Case Resistance	θ_{JC}	–	12	–	°C/W	2

Notes:

1. θ_{JA} measured in still-air room temperature test condition.
2. θ_{JC} measured with package held against an "infinite" heatsink test condition.

Table 16. Q2240I-2S1 and Q2240I-3S1 Operating Range

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Temperature (Ambient)	T_A	- 40	–	+ 85	°C	–
Operating Supply Voltage	V_{DD}	3.0	–	5.5	V	–
Junction to Ambient Resistance	θ_{JA}	–	32	–	°C/W	1
Junction to Case Resistance	θ_{JC}	–	15	–	°C/W	2

Notes:

1. θ_{JA} measured in still-air room temperature test condition.
2. θ_{JC} measured with package held against an "infinite" heatsink test condition.

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DC ELECTRICAL CHARACTERISTICS

Table 17 shows the DC electrical charcteristics for all of the Q2240 versions.

Table 17. DC Electrical Performance Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
High Level Input Voltage, TTL	V_{IH}	2.2	V_{DD} + 0.3	V	–
Low Level Input Voltage, TTL	V_{IL}	- 0.3	0.8	V	–
Input High Leakage Current, TTL	I_{IH}	- 10	+ 10	µA	1
Input High Leakage Current, TTL, 25 k Pull-down	I_{IHPD}	200	800	µA	1, 2
Input High Leakage Current, CMOS, 25 k Pull-down	I_{IHPD}	12.5	50	µA	1, 2
Input Low Leakage Current, TTL/CMOS	I_{IL}	- 10	+ 10	µA	3
Input Low Leakage Current, TTL, 25 k Pull-up	I_{IHPU}	- 800	- 200	µA	2, 3
High Level Output Voltage, CMOS (5 V)	V_{OH}	V_{DD} - 0.8	–	V	4
High Level Output Voltage, CMOS (3.3 V)	V_{OH}	V_{DD} - 0.5	–	V	4
Low Level Output Voltage, CMOS	V_{OL}	–	0.5	V	4
Quiescent I_{DD}	I_{DDQ}	–	100	µA	5
Power Dissipation @ Maximum SYS CLK (5 V)	P_D	–	2.0 @ 100 MHz	W	6
Power Dissipation @ Maximum SYS CLK (3.3 V)	P_D	–	0.5 @ 60 MHz	W	7

Notes:

1. Input = V_{DD} = V_{DDMAX}.
2. Refer to Tables 3, 4, 7, 10 and 11 for inputs equipped with internal pull-ups/pull-downs.
3. Input = V_{SS}, V_{DD} = V_{DDMAX}.
4. Refer to Tables 5, 8 and 12 for I_{OL}/I_{OH} currents (measured at V_{DDMIN}).
5. Inputs driven to V_{SS} or V_{DDMAX}. Measured at V_{DDMAX}.
6. For other clock frequencies,
   Power ≤ (15 mW/MHz) * (Clock Frequency) typical with ARBEN set "Low".
   Current ≤ (3 mA/MHz) * (Clock Frequency) typical.
7. For other clock frequencies,
   Power ≤ (6 mW/MHz) * (Clock Frequency) typical with ARBEN set "Low".
   Current ≤ (1.8 mA/MHz) * (Clock Frequency) typical.

TIMING SPECIFICATIONS

Figures 10 through 14 and Tables 18 through 25 show the timing specifications of the Q2240.

Figure 10. Q2240 Clock Interface Timing Diagram

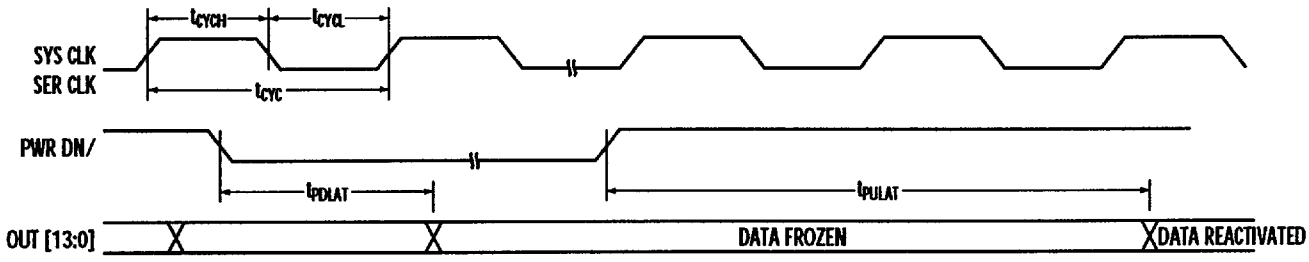

Table 18. Q2240I-1N Clock Interface Timing Specification

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{CYCL}	Minimum Low SYS CLK Pulse	9	–	ns
t_{CYCH}	Minimum High SYS CLK Pulse	11	–	ns
t_{CYC}	Minimum SYS CLK Period	20	–	ns

Table 19. Q2240I-2S1 and Q2240I-3S1 Clock Interface Timing Specification

SYMBOL	DESCRIPTION	MIN		MAX		UNITS	NOTES
		5 V	3.3 V	5 V	3.3 V		
t_{CYCL}	Minimum Low Clock Pulse	4.5	4.8	–	–	ns	1
t_{CYCH}	Minimum High Clock Pulse	4.5	4.8	–	–	ns	1
t_{CYC}	Minimum Clock Period	10	16.66	–	–	ns	2
t_{PDLAT}	Latency for Power-down	1* t_{CYC}		2* t_{CYC}		ns	3
t_{PULAT}	Latency for Power-up	2* t_{CYC}		3* t_{CYC}		ns	3

Notes:

1. Corresponding Duty Cycle Specification is 45%/55% for operation at 5 V; and 30%/70% for operation at 3.3 V.
2. Associated rise time requirement (10%-90%) for the leading edge of SER CLK is ≤ 15nsec.
3. t_{CYC} is the applied system clock (SYS CLK) period.

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Figure 11. Q2240I-1N and Q2240I-3S1 Asynchronous Parallel Interface (FCSELECT = "1") Timing Diagram

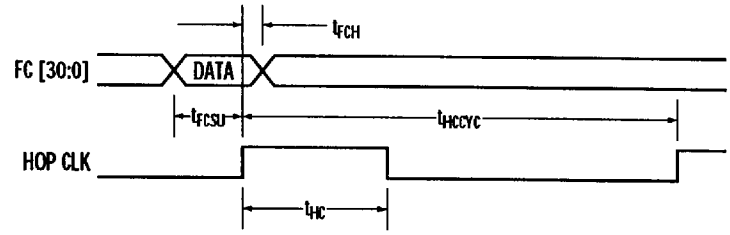

Table 20. Q2240I-1N and Q2240I-3S1 Asynchronous Parallel Interface Timing Specification

SYMBOL	DESCRIPTION	MIN		MAX		UNITS	NOTES
		5 V	3.3 V	5 V	3.3 V		
t_{FCSU}	FC Data Setup to Hop Clock Rising	3	3.5	–	–	ns	1
t_{FCH}	FC Data Hold After Hop Clock Rising	1.5	1.5	–	–	ns	1
t_{HC}	Hop Clock Minimum Pulse Width	t_{CYC} + 1		–		ns	2
t_{HCCYC}	Hop Clock Minimum Period	3* t_{CYC}		–		ns	2

Notes:

1. Specifications at 3.3 V operation apply only to the Q2240I-3S1 version.
2. t_{CYC} is the applied system clock (SYS CLK) period.

Figure 12. Q2240I-1N and Q2240I-3S1 Synchronous Parallel Interface (FCSELECT = "0") Timing Diagram

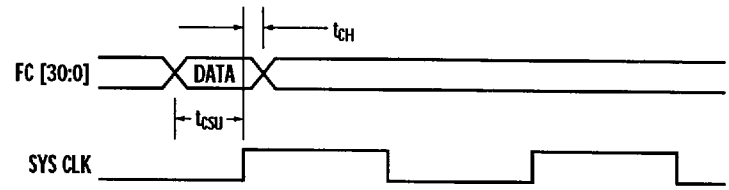

Table 21. Q2240I-1N and Q2240I-3S1 Synchronous Parallel Interface Timing Specification

SYMBOL	DESCRIPTION	MIN		MAX		UNITS	NOTES
		5 V	3.3 V	5 V	3.3 V		
t_{CSU}	FC Data Setup to SYS CLK Rising	3.5	4	–	–	ns	1
t_{CH}	FC Data Hold After SYS CLK Rising	1	1	–	–	ns	1

Notes:

1. Specifications at 3.3 V operation apply only to the Q2240I-3S1 version.

Figure 13. Q2240I-2S1 Serial Interface Timing Diagram

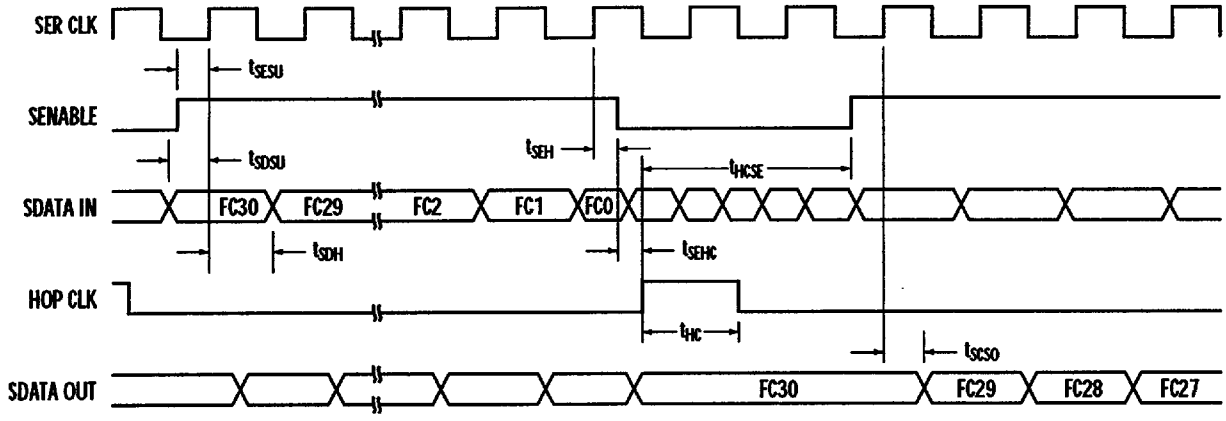

Table 22. Q2240I-2S1 Serial Interface Timing Specification

SYMBOL	DESCRIPTION	MIN		MAX		UNITS	NOTES
		5 V	3.3 V	5 V	3.3 V		
t_{SDSU}	Serial Data Setup to Serial Clock Rising	4	4.5	–	–	ns	–
t_{SDH}	Serial Data Hold After Serial Clock Rising	0	0	–	–	ns	–
t_{SESU}	Enable High Setup to Serial Clock Rising	5	7	–	–	ns	–
t_{SEH}	Enable High Hold After Serial Clock Rising	0	0	–	–	ns	–
t_{SCSO}	Serial Data Valid at SDATA OUT After SER CLK Rising	1.5	2.5	7	11	ns	–
t_{SEHC}	Hop Clock After SENABLE Falling	0	0	–	–	ns	–
t_{HCSE}	Next Enable High From Hop Clock Rising	$3* t_{CYC}$		–		ns	1
t_{HC}	Hop Clock Minimum Pulse Width	$t_{CYC} + 1$		–		ns	1

Notes:

1. t_{CYC} is the applied system clock (SYS CLK) period.

Figure 14. Q2240 Reset and Output Signals Timing Diagram

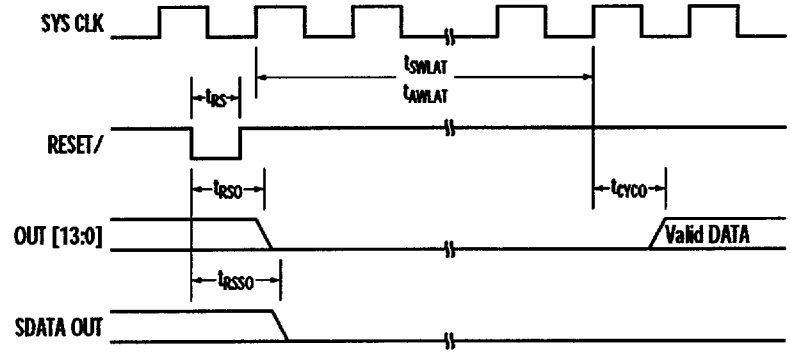

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Table 23. Q2240I-1N Reset and Output Signals Timing Specification

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
t_{RS}	Reset Pulse Width	10	–	ns	–
t_{RSO}	Reset to OUT [9:0] = 0	–	13	ns	–
t_{CYCO}	Clock to OUT [9:0]	1	7.5	ns	–
t_{SWLAT}	Latency for Valid Output at OUT [9:0]				
	When FCSELECT = "0"	14* t_{CYC}	14* t_{CYC}	ns	1
	When FCSELECT = "1"	16* t_{CYC}	17* t_{CYC}	ns	1

Notes:

1. t_{CYC} is the applied system clock (SYS CLK) period.

Table 24. Q2240I-2S1 Reset and Output Signals Timing Specification

SYMBOL	DESCRIPTION	MIN		MAX		UNITS	NOTES
		5 V	3.3 V	5 V	3.3 V		
t_{RS}	Reset Pulse Width	10	10	–	–	ns	–
t_{RSO}	Reset to OUT [13:0] = 0	–	–	13	20	ns	–
t_{RSSO}	Reset to SDATA OUT = 0	–	–	14	21	ns	–
t_{CYCO}	Clock to OUT [13:0]	1	1.5	7.5	12	ns	–
t_{AWLAT}	Latency for Valid Output at OUT [13:0] with Arbitrary Waveform Mode Enabled (ARBEN = "1")	12* t_{CYC}		13* t_{CYC}		ns	1
t_{SWLAT}	Latency for Valid Output at OUT [13:0] with Arbitrary Waveform Mode Disabled (ARBEN = "0")	16* t_{CYC}		17* t_{CYC}		ns	1

Notes:

1. t_{CYC} is the applied system clock (SYS CLK) period.

Table 25. Q2240I-3S1 Reset and Output Signals Timing Specification

SYMBOL	DESCRIPTION	MIN		MAX		UNITS	NOTES
		5 V	3.3 V	5 V	3.3 V		
t_{RS}	Reset Pulse Width	10	10	–	–	ns	–
t_{RSO}	Reset to OUT [13:0] = 0	–	–	13	20	ns	–
t_{CYCO}	Clock to OUT [13:0]	1	1.5	7.5	12	ns	–
t_{AWLAT}	Latency for Valid Output at OUT [13:0] with Arbitrary Waveform Mode Enabled (ARBEN = "1")						
	when FCSELECT = "0"	10* t_{CYC}		10* t_{CYC}		ns	1
	when FCSELECT = "1"	12* t_{CYC}		13* t_{CYC}		ns	1
t_{SWLAT}	Latency for Valid Output at OUT [13:0] with Arbitrary Waveform Mode Disabled (ARBEN = "0")						
	when FCSELECT = "0"	14* t_{CYC}		14* t_{CYC}		ns	1
	when FCSELECT = "1"	16* t_{CYC}		17* t_{CYC}		ns	1

Notes:

1. t_{CYC} is the applied system clock (SYS CLK) period.

QUICK REFERENCE FOR Q2220I-50N TO Q2240I-1N MIGRATION

FCSELECT INPUT

The FCSELECT input (pin 3) is used to select synchronous or asynchronous loading of the input frequency value (FC0 - FC22) into the FC Register, using either the system clock or HOP CLK signal, respectively. When left floating, the FCSELECT on the Q2220 would register as a logic "High" and therefore automatically set the Q2220 for activation by the HOP CLK signal. The Q2240I-1N does not have an internal pull-up resistor on its FCSELECT input. Therefore, a circuit that utilizes the device's FCSELECT input while left in a floating condition will have to connect a pull-up resistor from pin 3 to V_{DD} to ensure that the proper logic state is set for this control. (Typical pull-up resistor values are between 5 kΩ to 20 kΩ.)

RESET/ INPUT

The RESET/ input (pin 2) is used as an active "Low" asynchronous clear function. When left floating, the RESET/ on the Q2220 would register as a logic "High" and therefore automatically set the Q2220 to not be in a reset state. The Q2240I-1N does not have an internal pull-up resistor on its RESET/ input. Therefore, a circuit that utilizes the device's RESET/ input while left in a floating condition will have to connect a pull-up resistor from pin 2 to V_{DD} to ensure that the device does not hang in a reset state. (Typical pull-up resistor values are between 5 kΩ to 20 kΩ.)

NO CONNECT (N/C) PINS

Pins 19 and 20 for the Q2220 were specified as "No Connect" and therefore no electrical connection should be made to them. However, for the Q2240I-1N, pin 19 is tied internally to ground and pin 20 is tied internally to V_{DD}. These pins are still allowed to remain as "No Connect" with no external electrical connection without affecting the Q2240's operation. However, as a precaution, make sure that these pins are not inadvertently tied to any electrical connection that would affect the device.

POWER

The power consumption of the Q2240I-1N is rated at (15mW/MHz) * (Clock Frequency) versus the Q2220 which has a lower rating of (5 mW/MHz) * (Clock Frequency). This difference should be taken into account for the overall current consumption burden of the associated power supply, however, the Q2240I-1N will not require any special thermal management to sustain the rated operating junction temperature of less than +150°C.

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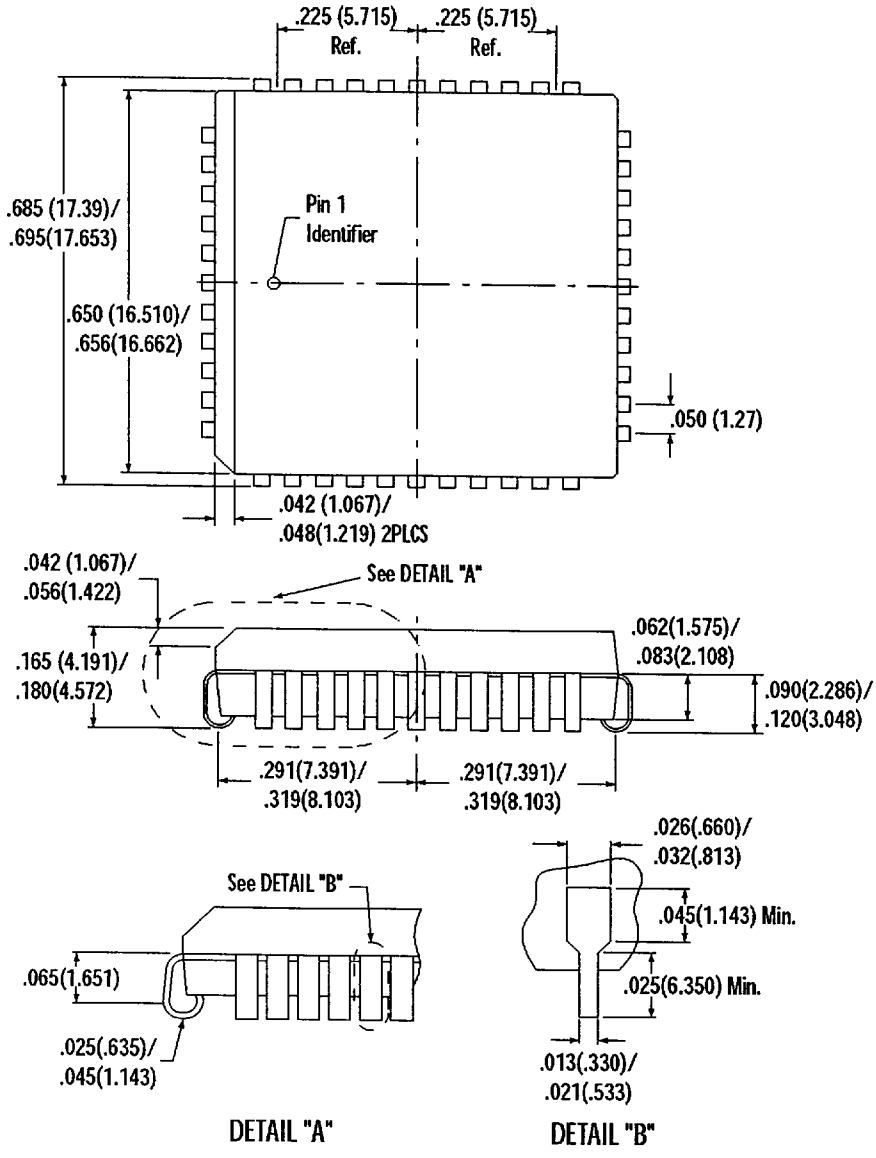
Q2240 PACKAGING

The Q2240I-1N comes in a 44-pin PLCC package which is shown in Figure 15. Figure 16 shows the package outline for the 64-pin PQFP package used for both the Q2240I-2S1 and Q2240I-3S1 versions.

Figure 15. Q2240I-1N 44-pin PLCC Package Outline



All dimensions are in inches (mm).

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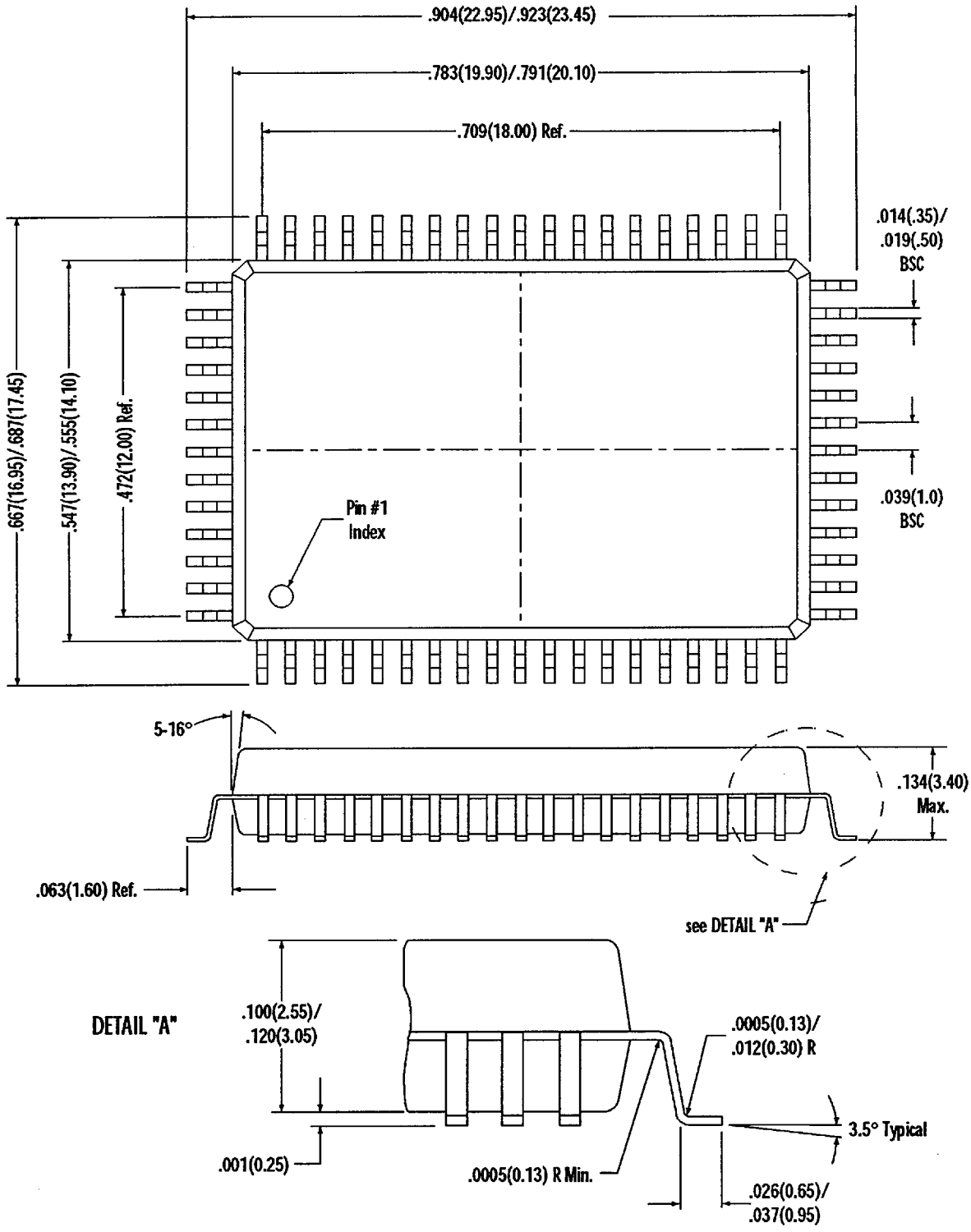
Figure 16. Q2240I-2S1 and Q2240I-3S1 64-pin PQFP Package Outline



All dimensions are in inches (mm).

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EVALUATION SYSTEMS FOR THE Q2240 DDSs

The Q0340-2 and Q0340-3 DDS Evaluation Systems were designed to demonstrate the capabilities and operating modes of the Q2240I-2S1 and Q2240I-3S1, respectively. The evaluation platform allows customers to evaluate either the Q2240I-2S1 or Q2240I-3S1 as a 5 V device operating at a maximum clock frequency of 100 MHz or as a 3.3 V device operating at a maximum clock frequency of 60 MHz. A block diagram of the Q0340-2 and Q0340-3 DDS Evaluation Systems are shown in Figure 17 and Figure 18. The evaluation board contains the associated Q2240 device coupled with a 100 MHz Digital-to-Analog Converter and the necessary analog output circuitry to provide optimum DDS performance. Both evaluation platforms are computer controlled through a digital I/O board that resides in the user's personal computer and Windows™ based software.

Alternatively, the Q0340-3 can be controlled through frequency control switches for stand-alone operation. The Control Software will automatically compute all desired frequency control words based upon the user's input and program the associated Q2240 DDS device. The User's Guide provides all information required to operate the Q0340-2 or Q0340-3. Appendices are also provided which contain the schematics, layout and complete parts list.

The Q0340-2 and Q0340-3 consist of a DDS Evaluation Board, Control Software, Control Cable, Digital I/O (DIO) Board and DIO Board Installation Software. In order to operate the DDS Evaluation Board, the DIO Board needs to be installed in a PC. The DIO Driver Software and the respective Control Software need to be installed on the hard drive of the PC. Both DDS Evaluation Systems require the following computer hardware as a minimum to operate in Remote Mode:

- PC 80386 or Better
- 4 MB RAM
- Math Co-processor
- Hard Drive
- Mouse
- Windows™ Version 3.1 or Windows '95™
- SVGA Video Card (1024 X 768 Resolution, Small Fonts)

Note: Windows™ is a trademark of Microsoft® Corporation.

Figure 17. Q0340-2 Functional Block Diagram

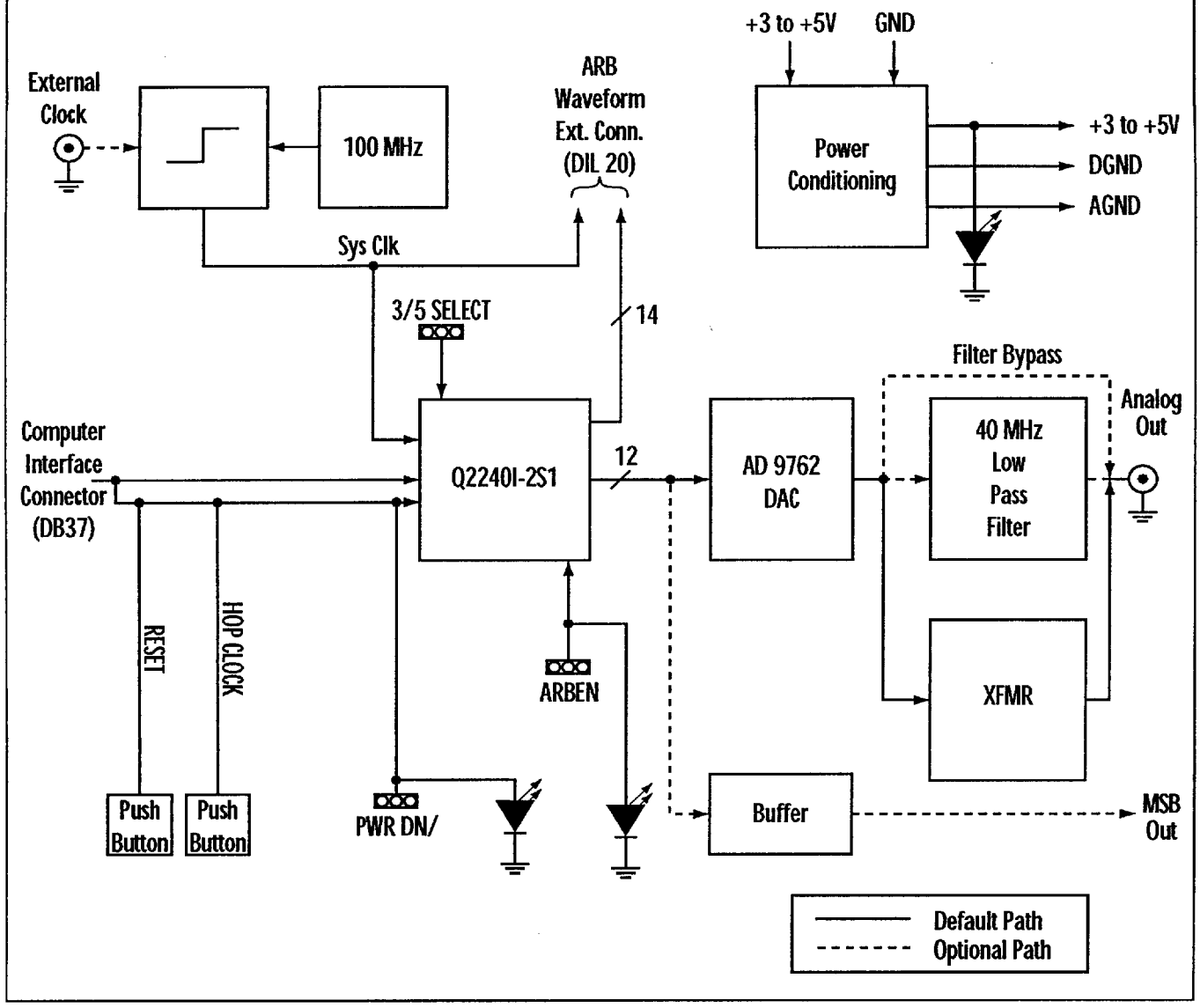

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Figure 18. Q0340-3 Functional Block Diagram