

15W Power Packaged Transistor

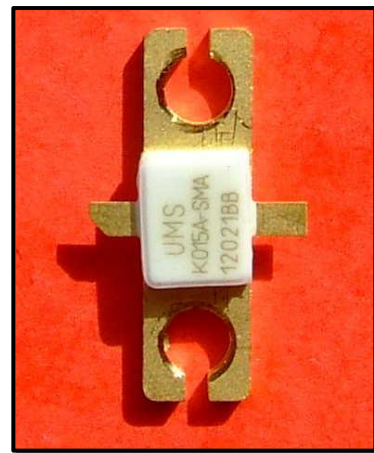
GaN HEMT on SiC

Description

The CHK015A-SMA is an unmatched packaged Gallium Nitride High Electron Mobility Transistor. It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication

The CHK015A-SMA is developed on a 0.5µm gate length GaN HEMT process. It requires an external matching circuitry.

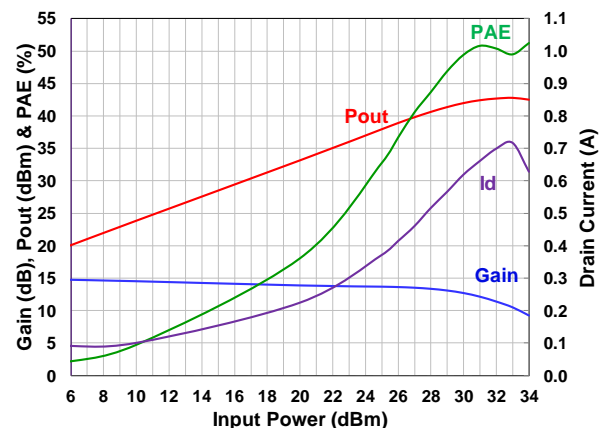
The CHK015A-SMA is available in a ceramic-metal flange power package providing low parasitic and low thermal resistance.



Main Features

- Wide band capability: up to 6GHz
- Pulsed and CW operating modes
- High power: > 15W
- High Efficiency: up to 70%
- DC bias: $V_{DS} = 50V$ @ $I_{D,Q} = 100mA$
- MTTF > 10^6 hours @ $T_j = 200^\circ C$
- RoHS Flange Ceramic package

$V_{DS} = 50V$, $I_{D,Q} = 100mA$, Freq = 5.6GHz
CW mode



Intrinsic performances of the packaged device

Main Electrical Characteristics

$T_{case} = +25^\circ C$, CW mode, $F = 5.6GHz$, $V_{DS} = 50V$, $I_{D,Q} = 100mA$

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain		15	-	dB
P_{SAT}	Saturated Output Power	15	18	-	W
PAE	Max Power Added Efficiency	45	50	-	%
G_{PAE_MAX}	Associated Gain at Max PAE		11	-	dB

Recommended DC Operating Ratings

T_{case}= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _{DS}	Drain to Source Voltage	20		50	V	
V _{GS_Q}	Gate to Source Voltage		-1.9		V	V _D = 50V, I _{D_Q} = 100mA
I _{D_Q}	Quiescent Drain Current		0.1	0.35	A	V _D = 50V
I _{D_MAX}	Drain Current		0.65	⁽¹⁾	A	V _D = 50V, Compressed mode
I _{G_MAX}	Gate Current (forward mode)		0	8	mA	Compressed mode
T _{j_MAX}	Junction temperature			200	°C	

⁽¹⁾ Limited by dissipated power

DC Characteristics

T_{case}= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _P	Pinch-Off Voltage	-3	-2	-1	V	V _D = 50V, I _D = I _{DSS} /100
I _{D_SAT}	Saturated Drain Current		2.7 ⁽¹⁾		A	V _D = 7V, V _G = 2V
I _{G_leak}	Gate Leakage Current (reverse mode)	-1			mA	V _D = 50V, V _G = -7V
V _{BDS}	Drain-Source Break-down Voltage		200		V	V _G = -7V, I _D = 20mA
R _{TH}	Thermal Resistance		6.4		°C/W	

⁽¹⁾ For information, limited by I_{D_MAX}, see on Absolute Maximum Ratings

RF Characteristics

T_{case}= +25°C, CW mode, F = 5.6GHz, V_{DS}=50V, I_{D_Q}=100mA

Symbol	Parameter	Min	Typ	Max	Unit
G _{SS}	Small Signal Gain	13	15	-	dB
P _{SAT}	Saturated Output Power	15	18	-	W
PAE	Max Power Added Efficiency	45	50	-	%
G _{PAE_MAX}	Associated Gain at Max PAE		11	-	dB

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB.

The typical performance achievable in more than 10% frequency band around 5.5GHz was demonstrated using the reference board 61499546 presented hereafter.

Absolute Maximum RatingsT_{case}= +25°C^{(1), (2), (3)}

Symbol	Parameter	Rating	Unit	Note
V _{DS}	Drain-Source Voltage	60	V	
V _{GS_Q}	Gate-Source Voltage	-10, +2	V	(6)
I _{G_MAX}	Maximum Gate Current in forward mode	25	mA	
I _{G_MIN}	Maximum Gate Current in reverse mode	-4	mA	
I _{D_MAX}	Maximum Drain Current	2	A	(4)
P _{IN}	Maximum Input Power (typical)	34	dBm	(5)
T _j	Junction Temperature	220	°C	
T _{STG}	Storage Temperature	-55 to +150	°C	
T _{Case}	Case Operating Temperature	See note	°C	(4)

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

⁽³⁾ The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may occur.

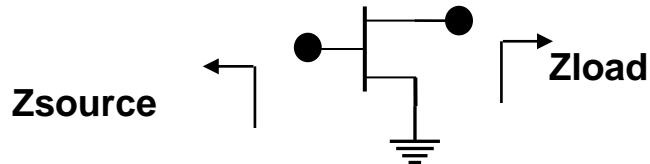
⁽⁴⁾ Max junction temperature must be considered

⁽⁵⁾ @6GHz - Linked to and limited by I_{G_MAX} & I_{G_MIN} values

⁽⁶⁾ V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values

Simulated Source and Load Impedance

$V_{DS} = 50V$, $I_{D_Q} = 100mA$



Frequency (MHz)	Source	Load
1000	$1.82 + j9.58$	$42 + j48.6$
2000	$0.84 - j1.53$	$13.8 + j25.7$
3000	$1.02 - j8.5$	$6.6 + j12.8$
4000	$1.86 - j15.82$	$5.1 + j2.6$
5000	$2.72 - j25.4$	$5.4 - j7.3$
6000	$2.87 - j41.14$	$6.7 - j17.2$

These values are given in the reference plane defined by the connection between the package leads and the PCB. A gap of $200\mu m$ is considered between the edge of the package and the PCB.

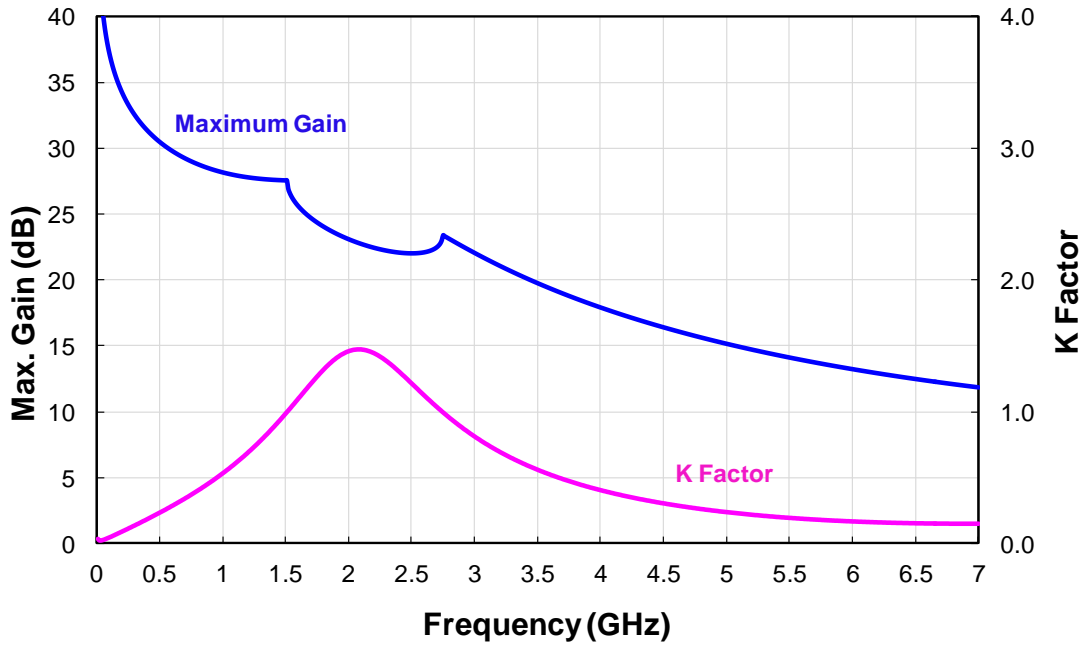
Typical S-parameters

T_{case}= +25°C, CW mode, V_D=50V, I_{D_Q}=100mA, Phase S(i,j) in °

Freq (GHz)	Mag S(1,1)	Phase S(1,1)	Mag S(2,1)	Phase S(2,1)	Mag S(1,2)	Phase S(1,2)	Mag S(2,2)	Phase S(2,2)
0.25	0.912	-82.5	30.268	129.4	0.014	42.4	0.649	-38.3
0.5	0.868	-123.0	19.526	102.4	0.017	18.4	0.542	-58.0
0.75	0.854	-143.5	13.768	85.8	0.017	5.2	0.517	-71.6
1	0.851	-156.0	10.431	73.3	0.017	-3.6	0.527	-83.4
1.25	0.852	-164.9	8.291	62.9	0.015	-9.6	0.551	-93.9
1.5	0.855	-171.9	6.814	53.6	0.013	-13.3	0.581	-103.5
1.75	0.859	-177.9	5.739	45.1	0.012	-14.3	0.612	-112.2
2	0.863	176.8	4.928	37.2	0.010	-11.7	0.641	-120.2
2.25	0.866	171.8	4.298	29.9	0.008	-4.0	0.668	-127.6
2.5	0.870	167.1	3.800	22.8	0.007	9.6	0.692	-134.5
2.75	0.872	162.5	3.401	16.2	0.008	26.2	0.714	-140.9
3	0.874	157.9	3.076	9.7	0.009	39.8	0.733	-146.9
3.25	0.875	153.3	2.809	3.4	0.011	47.8	0.750	-152.6
3.5	0.876	148.7	2.590	-2.7	0.014	51.4	0.764	-158.1
3.75	0.876	144.0	2.408	-8.7	0.017	52.2	0.776	-163.4
4	0.875	139.1	2.257	-14.7	0.020	51.2	0.786	-168.5
4.25	0.873	134.0	2.131	-20.6	0.024	49.0	0.794	-173.5
4.5	0.870	128.8	2.027	-26.6	0.027	45.9	0.801	-178.5
4.75	0.867	123.3	1.942	-32.7	0.032	42.3	0.807	176.6
5	0.863	117.4	1.872	-38.8	0.036	38.1	0.811	171.6
5.25	0.858	111.3	1.815	-45.2	0.040	33.4	0.814	166.6
5.5	0.853	104.7	1.770	-51.7	0.045	28.4	0.816	161.5
5.75	0.847	97.7	1.734	-58.5	0.050	22.9	0.818	156.2
6	0.841	90.2	1.707	-65.5	0.056	17.1	0.818	150.7
6.25	0.835	82.2	1.687	-73.0	0.061	10.8	0.818	144.9
6.5	0.829	73.6	1.672	-80.7	0.067	4.1	0.817	138.8
6.75	0.824	64.5	1.660	-89.0	0.073	-3.1	0.815	132.3
7	0.820	54.7	1.649	-97.6	0.079	-10.8	0.814	125.2
7.25	0.817	44.3	1.638	-106.8	0.086	-19.0	0.811	117.4
7.5	0.818	33.4	1.625	-116.5	0.092	-27.8	0.809	108.9
7.75	0.821	22.0	1.605	-126.8	0.097	-37.1	0.806	99.4
8	0.828	10.3	1.577	-137.7	0.102	-47.0	0.803	88.9
8.5	0.851	-13.5	1.486	-160.9	0.109	-68.4	0.799	64.3
9	0.883	-36.8	1.334	174.1	0.109	-91.5	0.802	34.9
9.5	0.915	-58.3	1.124	148.5	0.102	-115.2	0.819	2.6
10	0.940	-77.5	0.887	123.9	0.088	-138.1	0.849	-29.2
10.5	0.956	-93.8	0.663	101.6	0.072	-158.8	0.885	-57.4
11	0.966	-107.7	0.481	82.4	0.057	-176.8	0.916	-80.6
11.5	0.973	-119.4	0.346	66.3	0.045	167.7	0.94	-99.4
12	0.976	-129.5	0.249	52.7	0.035	154.0	0.956	-114.6
12.5	0.979	-138.2	0.182	41.4	0.028	141.6	0.966	-127.0
13	0.980	-145.9	0.135	31.9	0.023	130.1	0.972	-137.3
13.5	0.98	-152.7	0.101	23.9	0.019	119.0	0.975	-146.0
14	0.979	-158.8	0.078	17.1	0.016	108.5	0.975	-153.5
14.5	0.977	-164.3	0.061	11.5	0.014	98.7	0.975	-160.1
15	0.976	-169.4	0.049	6.7	0.012	90.0	0.974	-165.9

Maximum Gain & Stability Characteristics

T_{case}= +25°C, CW mode, V_D=50V, I_{D_Q}=100mA

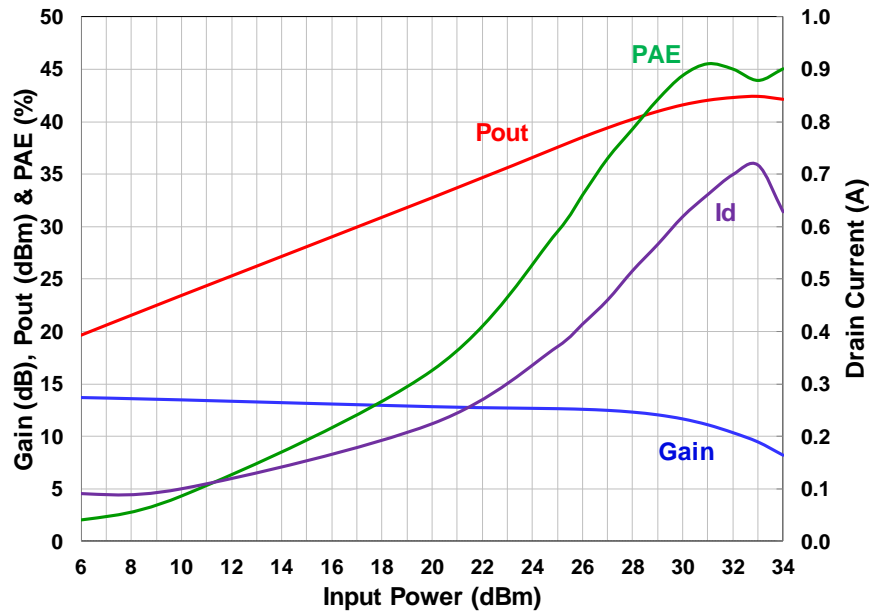


Typical Performance on Demonstration Board (Ref. 61499546)

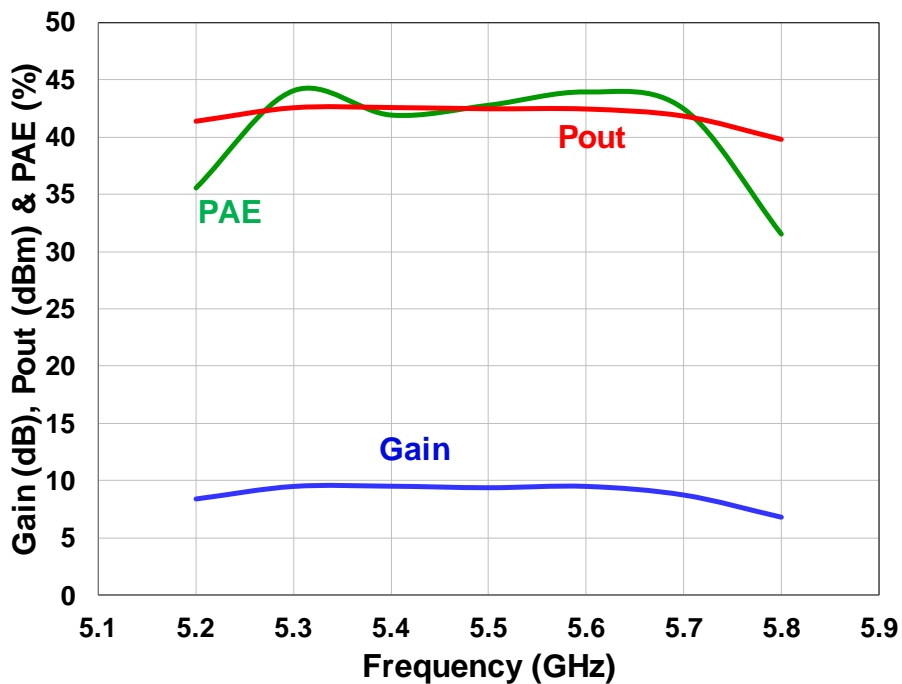
Calibration and measurements are done on the connector reference accesses of the demonstration boards.

T_{case} = +25°C, CW mode

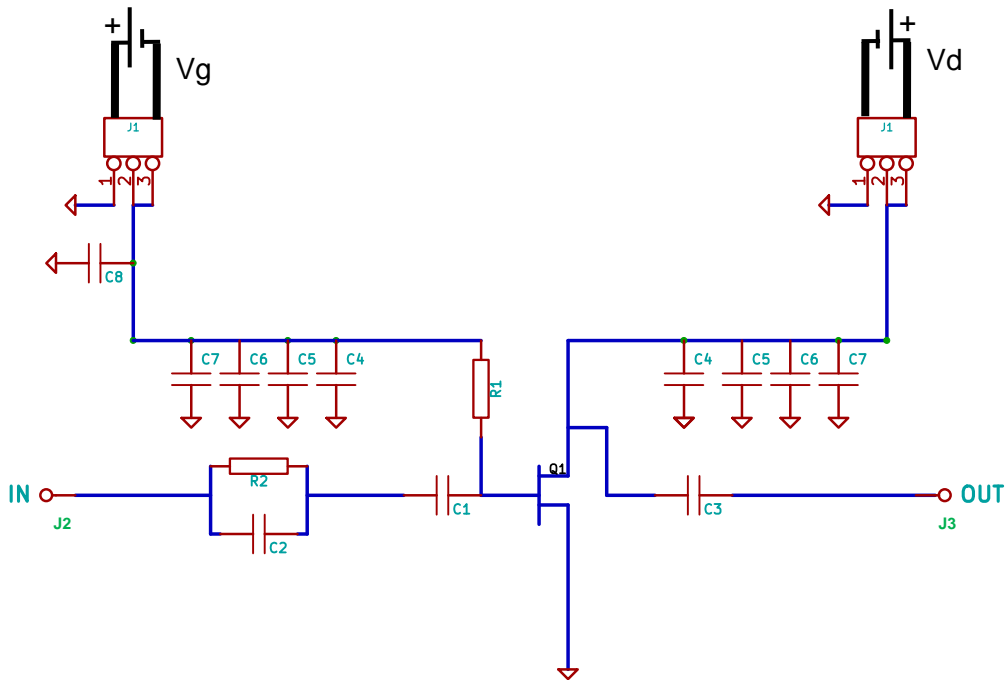
Measured Id, Pout, Gain & PAE
 F = 5.6GHz, V_{DS} = 50V, I_{D_Q} = 100mA



Measured Pout, Gain & PAE
 Pin=33dBm, V_{DS} = 50V, I_{D_Q} = 100mA



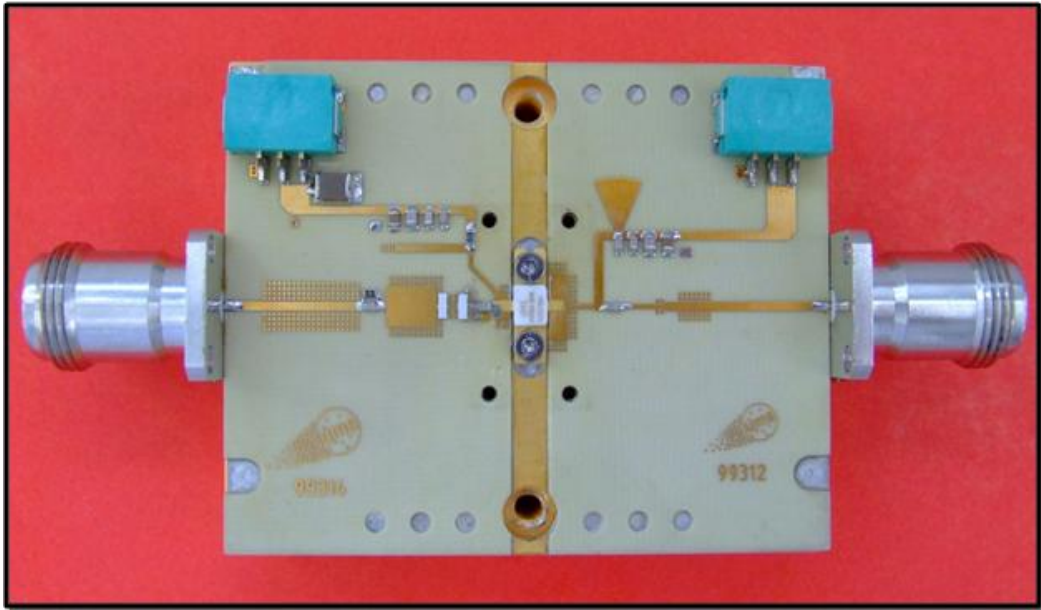
Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61499546)



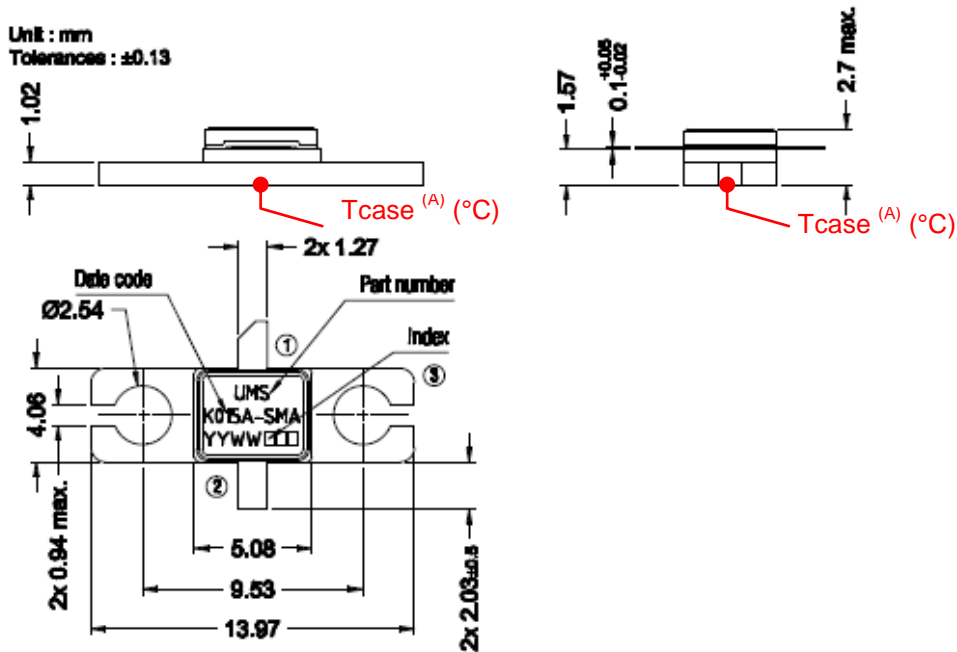
Demonstration Amplifier / Bill of Materials (Ref. 61499546)

Designator	Type	Value - Description	Qty
C1	Capacitor	0.2pF, +/- 0.05pF, 0603	1
C2	Capacitor	1.2pF, +/- 0.1pF, 0603	1
C3	Capacitor	2pF, +/- 0.1pF, 0603	1
C4	Capacitor	18pF, +/- 5%, 0603	2
C5	Capacitor	39pF, +/- 5%, 0805	2
C6	Capacitor	180nF, +/- 5%, 0805	2
C7	Capacitor	10nF, +/- 5%, 0805	2
C8	Capacitor	1µF, +/- 10%, 1204	1
R1	Resistor	360Ω, +/- 1%, 0603	1
R2	Resistor	220Ω +/- 1%, 0603	1
J1	Connector	CMS 3cts	2
J2, J3	Connector	N	2
Q1	Packaged Transistor	CHK015A-SMA	1
-	PCB	RO4003, Er=3.55, h=0.508mm	-

Demonstration Amplifier Circuit (Ref. 61499546)



Package outline



**PIN-OUT: 1- GATE
2- DRAIN
3- SOURCE (Gnd)**

(A) Tcase locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.

(B) Chamfered lead indicates the gate access of the packaged transistor.

Recommended Assembly Procedure

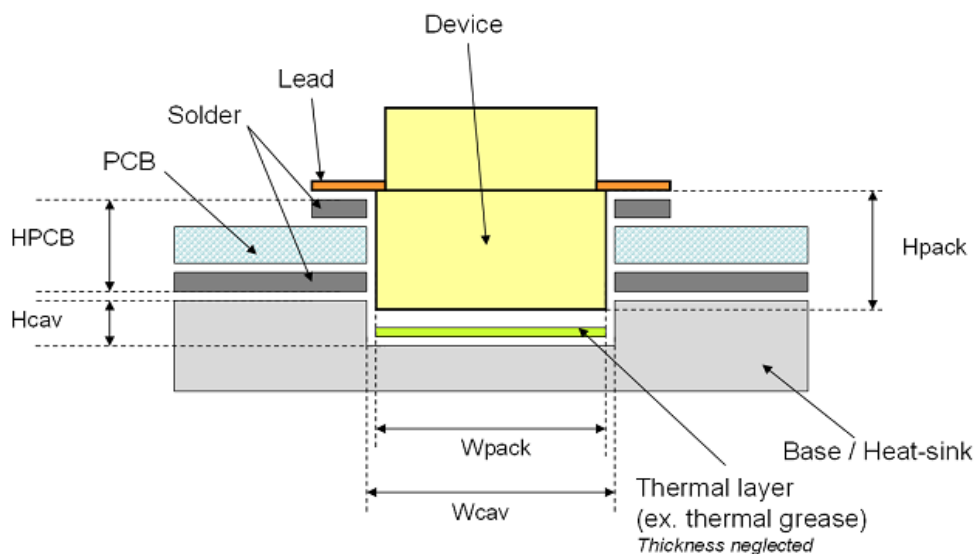
CHK015A-SMA is available has a flange package to be bolt down onto a thermal heat sink also used as main electrical ground. Use preferably screw M2 and flat washers.

Thermal and electrical resistance at the package to heat sink interface has to be as low as possible. Thermal electrically conductive grease or conductive thin layer like indium sheets are recommended between the package and the heat sink.

In case a thermal grease is selected, we recommend to use material offering thermal conductivity $>5\text{W/m.K}$ and electrical resistivity $<0.01\text{ ohm.cm}$. The grease layer thickness should be about $25\mu\text{m}$ (1 mil).

Contact interface quality can be improved by cleaning process prior device mounting on the heat-sink. Such operation will enhance the thermal and electrical contact by oxide removal at each interface.

Package leads can be soldered on printed circuit board's traces by using RoHS solder past. Cavity depth and width to be performed into the heat-sink where the device will be mounted are important to achieve the best performances. These dimensions have to be optimized in order to minimize the distance between device and signal traces made on the printed circuit board (PCB). But they also have to be calculated in order to accommodate device variations in height. The following drawing gives the relationship between device dimensions (H_{pack} & W_{pack}) and optimal cavity depth (H_{cav}) and width (W_{cav}) depending on the printed circuit-board configuration (H_{PCB})



$$H_{\text{cav}} = (H_{\text{pack}_{\text{min}}} - H_{\text{PCB}_{\text{max}}})^{+0}_{-0.05}$$

$$W_{\text{cav}} = (W_{\text{pack}_{\text{max}}} + 0.4)^{+0}_{-0.05}$$

dimensions are in mm

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Package: CHK015A-SMA/XY
Tray: XY = 26

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